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A finite state machine read-out chip for integrated surface acoustic wave sensors

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ABSTRACT

A finite state machine based integrated sensor circuit suitable for the read-out module of a monolithically integrated SAW sensor on Si is reported. The primary sensor closed loop consists of a voltage controlled oscillator (VCO), a peak detecting comparator, a finite state machine (FSM), and a monolithically integrated SAW sensor device. The output of the system oscillates within a narrow voltage range that correlates with the SAW pass-band response. The period of oscillation is of the order of the SAW phase delay. We use timing information from the FSM to convert SAW phase delay to an on-chip 10 bit digital output operating on the principle of time to digital conversion (TDC). The control inputs of this digital conversion block are generated by a second finite state machine operating under a divided system clock. The average output varies with changes in SAW center frequency, thus tracking mass sensing events in real time. Based on measured VCO gain of 16 MHz/V our system will convert a 10 kHz SAW frequency shift to a corresponding mean voltage shift of 0.7 mV. A corresponding shift in phase delay is converted to a one or two bit shift in the TDC output code. The system can handle alternate SAW center frequencies and group delays simply by adjusting the VCO control and TDC delay control inputs. Because of frequency to voltage and phase to digital conversion, this topology does not require external frequency counter setups and is uniquely suitable for full monolithic integration of autonomous sensor systems and tags.

1. Introduction

Typically, readout modules for vapor and liquid phase SAW sensors fabricated on piezoelectric films are configured as single or dual delay line oscillator loops [10–13]. Mass loading of the sorbent film realized on the SAW device is detected as a frequency shift which is read externally via a frequency counter. However, this approach is not directly applicable in the development of a monolithically integrated autonomous sensor system suitable for wearable sensor tags and other field applications. The motivation of this work is to present an alternate read-out topology for an integrated CMOS SAW sensor which achieves closed loop conversion of the SAW frequency response to a well defined output voltage accurately tracking sensor behavior in real time. This design uses a finite state machine (FSM) to control the VCO. In previous work the authors presented a topology of the primary sensor loop [3]. In this work the design is expanded to efficiently convert the sensor output to a digital readout. This is accomplished by using the timing information embedded in the existing FSM outputs and adding a second FSM in the conversion circuit. This topology avoids loss of resolution resulting from buffering of the analog signal for use in switched capacitor based conversions. Our readout topology is best targeted for low loss interdigitated (IDT) SAW sensors, such those reported in Krishnamoorthy and Iliadis [1] and [2], that have high electromechanical coupling coefficient (k^2). Additionally, this low frequency loop architecture (Fig. 1) precludes mode jumping issues found in designs incorporating the SAW delay line or the resonator in the feedback loop of an amplifier [9]. In the following sections the design, simulation and experimental verification of the FSM based frequency-to-voltage conversion read-out IC circuit will be presented and discussed.

2. Top level architecture

The FSM based read-out is implemented in two layers. The communication between the two layers occurs via the FSM and the comparator outputs. The primary loop sensor loop block diagram is shown in Fig. 1. When the loop is closed as shown, the VCO output frequency varies between limits dependent on the device passband, the SAW phase delay, the RC filter time constant and the VCO gain. The SAW output frequency is centered at the upper edge of the passband. This output is fed to a peak detecting comparator with

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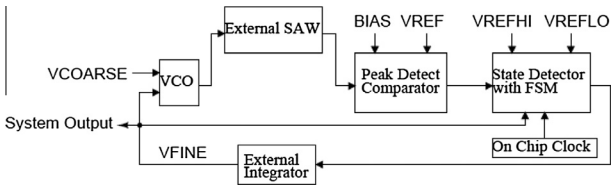

Fig. 1. Primary sensor loop block diagram.

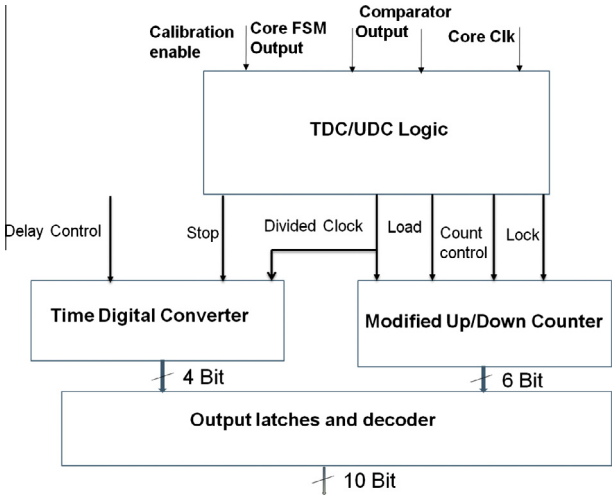

Fig. 2. Digital conversion of sensor output.

hysteresis whose output is high if the frequency is in the passband. Each toggle of the comparator output causes the VCO ramp input to reverse slope and this, in turn causes the VCO output frequency to enter and exit the passband. The average value of the VCO fine ramp thus serves as the system output. Two additional comparators provide reset and clear functionality to bring the ramp to the working band from its initial high or low state. A finite state machine ensures correct transitions between states.

In the second layer of conversion, the analog sensor output is converted to an equivalent 10 bit digital output. The block diagram of this read-out phase is shown in Fig. 2. The FSM and comparator outputs from the primary sensor loop are fed into a digital control logic block which generates control inputs for a 4 bit time to digital converter (TDC) and a 6 bit modified up/down counter (UDC). The UDC counts up or down when the comparator output is high while remaining locked at other times. The TDC provides a finer resolution of the delay from the count clock to the comparator output. Combining these two digital buses, we obtain a digital representation of the total charge up time of the external filter. As derived in [3], the average sensor output is a function of this charge up time.

3. Readout operation

The primary loop FSM which acts as the conduit between the two layers receives an input from the peak detecting comparator which detects if the instantaneous SAW frequency is in the passband. The comparator node transition diagram is shown in Fig. 3. Shown in Fig. 4 is the state transition diagram for the detector. Six states are observable here. In all cases a transition is contingent on a change in the comparator output and the current state of the FSM. In state S1, the instantaneous SAW output frequency is below the passband and the instantaneous VCO output frequency is increasing. Note that the SAW delay line imposes a delay between the time varying frequencies at the SAW output and the VCO output. In S2 the SAW output frequency is within the passband and the VCO output frequency is increasing. A transition from this state is induced when the SAW output frequency exits the passband causing the comparator output to go low. In S3 the SAW output frequency is above the passband and the VCO output frequency is

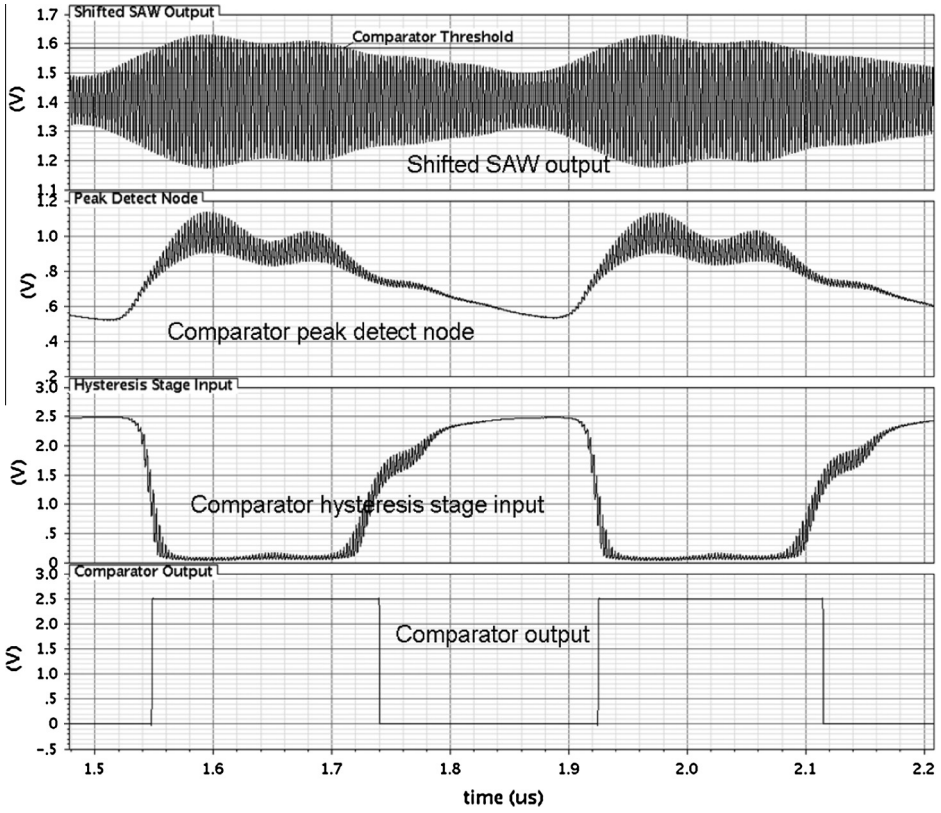

Fig. 3. Comparator node transitions.