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Model of current-limited negative differential resistance in oxide-based resistance-switching devices

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ABSTRACT

Resistance-switching devices such as resistive random access memories (RRAMs) exhibit the ability to rapidly reduce resistance upon exceeding a threshold voltage, as part of the SET operation. For oxide-based RRAMs, the progressive generation of defects during SET requires strict regulation of the current, e.g., by a transistor, in order to avoid irreversible breakdown. In doing so, the current-limiting device itself takes some voltage burden. The observed negative differential resistance for both the initial (forming) and regular SET operations can be analytically explained with a basic circuit model for the current-limited switching element, linking the voltage transfer to the current-limiting device with the degree of current rise. Consequently, it is found that RRAM operation current is a vital consideration for the reliability of the current-limiting device.

1. Introduction

RRAM technology has received much attention recently, due to the simpler fabrication process, lower voltage operation, higher operation speed, and higher endurance, compared to the floating-gate flash as the current mainstream non-volatile memory. In an oxide-based RRAM, the SET operation is associated with the generation of oxygen vacancies, which allow conduction paths ('filaments') to be formed under an applied bias, leading to a reduction in resistance. On the other hand, the RESET operation is associated with the interruption of these paths, through the elimination of vacancies, also upon application of a voltage bias, often in the opposite polarity.

Many oxide-based RRAMs initially start in an insulating state, and therefore require a forming operation, essentially an initial SET operation, that generates in one step a sufficient number of oxygen vacancies for the switching to low resistance to proceed. However, this operation is characterized by internal runaway current, which could lead to a permanent breakdown. Thus, a compliance setting must be applied to limit the current from rising above a given level. The compliance current level setting is a key aspect in determining the switching behavior of RRAMs, including multi-level cell (MLC) operation [1]. This compliance may come from an external tester, a series resistor, an on-chip transistor, or a novel integrated two-terminal selector device (Fig. 1). Actually, for the current-limiting device to work, a voltage must be applied across it, and this voltage actually is transferred from the oxide at the onset of forming. The forming voltage can be quite large (>5 V) so that when transferred to the current limiter, it could irreparably damage it. Therefore, it will be very useful to have an analytical model that predicts how much voltage is transferred to the current limiter during forming. Up to now, such a model has not been presented.

In this paper, the voltage transfer is shown to be related to the negative differential resistance (NDR) which can be observed in the *I–V* curve of the resistance-switching element. A rigorous analysis of the NDR is provided as well.

2. Materials and methods

The RRAM devices used in this work are fabricated as 0.4 μm diameter stacks comprising a TiN bottom electrode, a nominally 5 nm thick HfO_x layer deposited by atomic layer deposition on the bottom electrode, a nominally 5 nm thick Ti layer, capped by a TiN top electrode. The current was regulated with foundry-provided NMOS transistors with $W/L = 4.8\ \mu m/0.35\ \mu m$, in series with the RRAM element, forming a one-transistor one-resistor (1T1R) cell. Fig. 2 shows a representation of the device being tested.

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3. Experimental

A sweep rate of 0.1 V/0.1 s is used to obtain the *I–V* curves used for this work. A direct connection to the transistor drain enabled the collection of the I_{ds}–V_{ds} curve for the same transistor used in obtaining the 1T1R *I–V* curve. This allowed the *I–V* curve for the resistance-switching element by itself to be obtained. Fig. 3 shows the method of extraction.

4. Theory

Fig. 4 shows the general setup for current-limited RRAM testing. The resistance-switching element is represented by the resistance R_r, in parallel with a parasitic capacitance C_{pr} (typically on the order of 1 fF). A current-limiting resistance (e.g., the channel of a transistor) R_t, along with a parasitic capacitance C_{pt} (typically on the order of 0.1 fF) in parallel with R_t, is connected in series with the R_r–C_{pr} combination. The impact of parasitic capacitances has been indicated in previous work [2,3] but here the specific voltage shifts between switching resistance and current limiter during the current-limited forming and SET operations will be explored.

4.1. Mild NDR ($R_r \gg R_t$): negligible transition

For the case where R_r does not vary significantly, the analysis of the circuit of Fig. 4 is quite straightforward. We first assume R_r is constant during the time interval $t = 0$ to $t = t_0$ (e.g., $t_0 \ll R_rC_{pr} \sim 1$ ns for $R_r \sim 1\ \mathrm{M}\Omega$, $C_{pr} \sim 1$ fF) we relate the charge on C_{pr} to the current I_r through R_r:

$$\frac{Q_{pr}}{C_{pr}} = I_rR_r, \tag{1}$$

and likewise for C_{pt} and I_t:

$$\frac{Q_{pt}}{C_{pt}} = I_tR_t, \tag{2}$$

the total current I through R_t is related to I_r and the displacement current through C_p by:

$$I_t + \frac{dQ_{pt}}{dt} = I_r + \frac{dQ_{pr}}{dt}. \tag{3}$$

The fixed applied voltage V_s is related to I_r and I_t through the sum of the respective voltage drops on the resistance-switching element and current-limiting element, respectively:

$$V_s = I_tR_t + I_rR_r. \tag{4}$$

Combining (1)–(4) yields a differential equation for I_r:

$$\frac{dI_r}{dt} + \frac{1+\frac{R_r}{R_t}}{R_rC_{pr}+R_tC_{pt}}I_r = \frac{\frac{V_s}{R_t}}{R_rC_{pr}+R_tC_{pt}} + \frac{d}{dt}\left(\frac{C_{pt}V_s}{R_rC_{pr}+R_tC_{pt}}\right), \tag{5}$$

with the solution given by:

$$I_r = \frac{V_s}{R_t+R_r} + \left(I_r(t=0) - \frac{V_s}{R_t+R_r}\right)\exp\left(-\frac{t}{\tau}\right), \tag{6}$$

where

$$\tau = \frac{R_rC_{pr}+R_tC_{pt}}{1+\frac{R_r}{R_t}}. \tag{7}$$

$I_r(t = 0)$ is in fact determined by the initial voltage drop on R_r, V_r, since the voltage on the capacitance C_{pr} must be continuous. At least for initial SET or forming, V_r is taken to be V_s, and $R_r \gg R_t$. Since R_r does not vary during this transition, the initial I_r is given by:

$$I_r(t=0) = \frac{V_r}{R_r} = \frac{V_s}{R_r}. \tag{8}$$

Substituting this back into (6) and recalling $R_r \gg R_t$, we get:

$$I_r = \frac{V_s}{R_r}. \tag{9}$$

In other words, there is no transient current since R_r is constant and much higher than the series resistance R_t. This conclusion also holds if R_r decreases, but not abruptly. At time $t = t_0$, R_r may vary slightly to a value $R_r - \delta R$ and the analysis may be repeated, arriving at the same solution (6), but with R_r replaced by $R_r - \delta R$ in (6)–(9), and the time variable t being replaced by $t' = t - t_0$.

4.2. Aggressive NDR ($R_t \gg R_r$): abrupt transition

Let us now consider the extreme opposite case, where R_r, although initially high, suddenly drops to a very low value R_0, i.e., $R_0 \ll R_t$. In this case, (5) still holds, and the solution (6) becomes:

$$I_r = \frac{V_s}{R_t} + \left(\frac{V_s}{R_0} - \frac{V_s}{R_t}\right)\exp\left(-\frac{t}{\tau}\right) = \frac{V_s}{R_t} + \frac{V_s}{R_0}\exp\left(-\frac{t}{\tau}\right), \tag{10}$$

which clearly indicates a transient current with maximum amplitude of $\sim V_s/R_0$. Note here that R_0 is independent of R_t. Furthermore, since $R_0 \ll R_t$, at steady state ($t \gg \tau$), $V_r \ll V_t \sim V_s$, i.e., all the voltage V_s is transferred in its entirety to the current-limiting device, at which point no energy is dissipated in the resistance-switching element itself. This situation is not consistent with the ability to perform MLC operation by regulating R_t [1].

4.3. General case: continuous transition

For the general case of RRAM switching during the SET or forming operation the NDR is expected to lie in between the extreme cases described in Sections 4.1 and 4.2. We may model the evolution of R_r by multiple mild decreases of R_r (Fig. 5) between different time intervals $[0,t_0]$, $[t_0,t_1]$, etc., generalizing from the results of Section 4.1.

In this case, we may apply the solution (4) for each time interval. Each time interval is expected to be ultra-short (≪ns). Initially, when R_r is high, the results of the mild NDR case will apply, resulting in a sequence of different initial current amplitudes V_s/R_{r1}, V_s/R_{r2}, etc. for the transients corresponding to each interval. Eventually V_r will decrease below V_s, eventually approaching 0.

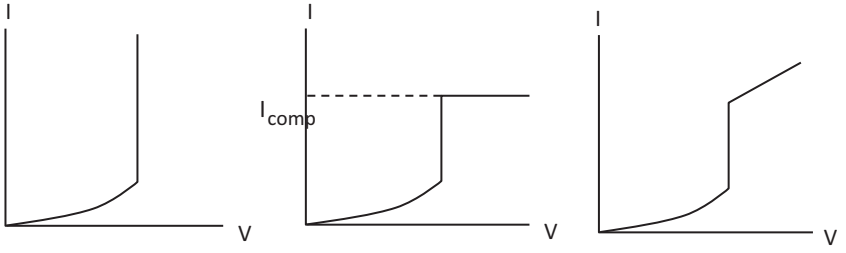

Fig. 1. Different cases of current compliance. Left: no compliance, center: transistor-limited compliance (saturation mode), right: resistor-limited compliance.