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50 nm Al_xO_y ReRAM program 31% energy, 1.6× endurance, and 3.6× speed improvement by advanced cell condition adaptive verify-reset

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ABSTRACT

Two verify-reset schemes are proposed to improve the program energy, endurance and speed of 50 nm Al_xO_y ReRAM cells. Both of the proposed schemes improve the verify-reset program by adapting the program voltage and pulse width to the variation of ReRAM cell filament status during the verify-reset. In this paper, first, the reset resistance and cell endurance are compared using different reset voltages and reset pulse widths. Then, two proposed verify-reset schemes are introduced independently. The first proposed scheme *controlled reset voltage* (V_{reset}) *increment* demonstrates 32% program energy reduction and 6.7× program speed increase. In this scheme, the reset voltage stress is increased from −1.5 V to −1.65 V, only when the reset-tries fail continuously during verify-reset (hard-to-reset). The second proposed scheme *set-before-reset* applies the set pulse during verify-reset, to convert the filament from a hard-to-reset state to an easy-to-reset state. With this approach, 31% program energy reduction, 1.6× program endurance and 3.6× program speed increase can be obtained simultaneously.

1. Introduction

Transition metal oxide based resistive random access memory (ReRAM) is considered a promising next generation non-volatile memory technology due to its capability of fast speed, low power program and the scaling potential [1–4]. Various materials can be used as the resistance switching layer and electrode. By investigating their resistance switching properties [1–15], the ReRAM with the Al_xO_y layer and the ReRAM doped with Al_xO_y are found having favorable characteristics of improved resistance uniformity [9,10] and lower program current, which have been proved both theoretically [11–13] and experimentally [8,9,14,15], compared with using other resistance transition materials, e.g. HfO_x, TiO_x, TaO_x, and NiO_x.

The resistance decrease and increase of the transition metal oxide based ReRAM cell can be attributed to the formation and rupture of the oxygen vacancy (V_o) filament [1]. In detail, after a set pulse, the filament can be formed to decrease the cell resistance (R_{set}) to a low resistance state (LRS). In contrast, the filament can be ruptured after a reset pulse to increase the cell resistance (R_{reset}) to a high resistance state (HRS). To ensure a sufficient resistance margin between the HRS and LRS, the verify-set and verify-reset (verify-program) schemes should be used [16], in which the operations of program pulse and resistance read are repeated until the cell resistance reaches the target resistance region. Furthermore, the set current increment and reset current reduction can be found during the resistance transition. To improve the verify-program, the research in [17] uses an external control circuit on a ReRAM array, to detect the current variation and terminate the program stress right after the resistance transition completes. In this way, by comparing with their conventional verify-program, the cell endurance is improved due to the elimination of the excessive program stress, which may cause a local high temperature on the ReRAM cell and decreases the density of movable oxygen vacancies [17]. As for the disadvantage of this method, monitoring the program current can be cumbersome because of the extra circuit area, which may limit the number of bits that can be programmed in parallel. Therefore in [18] the prior work improves the Al_xO_y ReRAM cell endurance and program energy by using a proposed verify-reset and verify-set schemes (introduce in Section 3). The

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improved schemes in [18] are considered as the conventional scheme of this paper.

In the rest of this paper, the detail of experiment is explained in Section 2. Section 3 introduces the conventional verify-program scheme. In Section 4, first, the cell endurance and R_{reset} are compared by using the conventional verify-program scheme with different reset voltages and pulse widths. Then, the first proposed verify-reset scheme *controlled reset voltage* (V_{reset}) *increment* is introduced to improve the cell endurance and program energy. In this scheme, the reset voltage stress is increased during verify-reset only when the reset-tries fail continuously (hard-to-reset). At last in Section 5, the program endurance, energy and speed are improved at the same time by using the second proposed verify-reset scheme *set-before-reset*. In this scheme, the set pulse is applied during verify-reset to convert the filament from a hard-to-reset state to an easy-to-reset state. Therefore, the ReRAM cell can reset with faster speed and smaller energy. In [19], a similar proposal can be found using the idea of reversed voltage during verify-program. However, the scheme and mechanism are different in the proposal compared with in the *set-before-reset*. First in [19], the TaO_x ReRAM has a hard-to-set problem so that a "reset-before-set" scheme is used. Second, though the reset pulse normally increases the cell resistance, it also decreases the cell resistance when it is hard-to-set. The bi-directional resistance change using the reset pulse shows a different mechanism compared with the *set-before-reset* scheme.

2. Experiment

The structure of 50 nm Al_xO_y ReRAM cell is shown in Fig. 1(a) [18]. The ReRAM cell is attached with a NMOS transistor to limit the program current. To measure this cell, the resistance read is applied on V_d by a semiconductor parameter analyzer. The set and reset pulses are generated by an arbitrary function generator. The typical set and reset pulse waveforms are shown in Fig. 1(b) [18]. The set pulse has the voltage V_{set} = 2.5 V and pulse width T_{set} = 100 ns. It is applied on the V_d to decrease the cell resistance to LRS. In contrast, the reset pulse has an opposite voltage polarity V_{reset} = −1.5 V with pulse width T_{reset} = 20 ns. It is also applied on the V_d, but to increase the cell resistance to HRS. The target LRS and HRS resistances are $R_{set} \leqslant 5 \times 10^4\,\Omega$ and $R_{reset} \geqslant 2 \times 10^5\,\Omega$, respectively. The substrate voltage of this transistor is controlled independently to prevent the junction leakage during program. For both set and reset programs, the NMOS substrate always has the lowest voltage. During set, the substrate voltage is V_{sub} = 0 V, and the typical drain voltage is V_d = 2.5 V. During reset, the typical $V_{sub} = V_d = -1.5$ V (the reset voltage V_d can be changed, but the V_{sub} equals to the V_d during reset program).

3. Conventional verify-program scheme

Fig. 2 shows the cell endurance test flow [18]. After forming, the endurance measurement loop is operated including the accelerated programs, verify-reset and verify-set. After that, the initial reset pulse width (T_{init_reset}) and initial set voltage (V_{init_set}) are changed for the next endurance measurement loop. For the detail of the endurance measurement loop, the reset and set pulses are repeated 4000 times in the accelerated programs (without verify-program or resistance read) to accelerate the endurance measurement. Then, during the verify-reset, the reset program pulse and resistance read are repeated until the cell is at HRS state. In detail, as the number of applied reset program pulse m increases, the T_{reset} is increased from the initial reset pulse width T_{init_reset}, to provide stronger reset strength [18]. The V_{reset} is fixed because the high V_{reset} stress accelerates the cell break [20]. For the verify-set, the voltage increment scheme is found more effective to decrease the cell resistance [20]. In detail, the V_{set} is increased from the initial set voltage V_{init_set} with the incremental step 0.1 V. The cell is considered break if the cell fails to reset or set within 21 pulses [18]. At last, the initial reset pulse width T_{init_reset} and the initial set voltage V_{init_set} are modified for the next endurance measurement loop to adapt the cell wear-out. It can be found from both

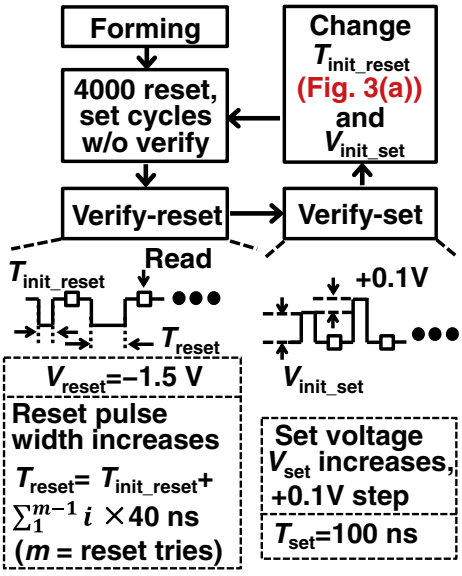

Fig. 2. The endurance test flow [18]. After forming, the endurance measurement loop is operated including the accelerated programs, verify-reset and verify-set. After that, the initial reset pulse width (T_{init_reset}) and initial set voltage (V_{init_set}) are changed for the next endurance measurement loop.

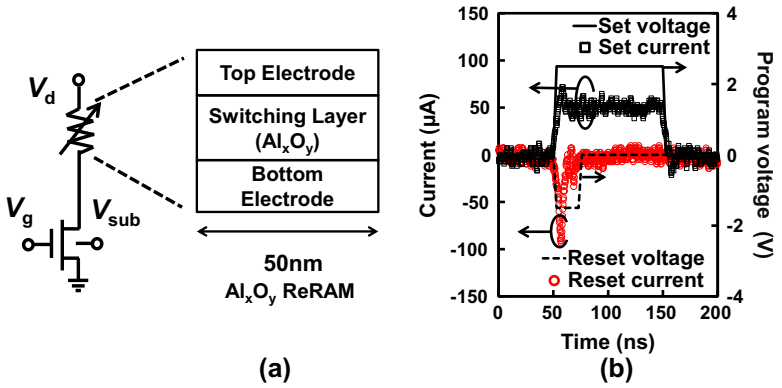

Fig. 1. (a) The 50 nm Al_xO_y ReRAM cell structure [18]. (b) The waveforms of a typical set pulse and reset pulse [18].