Solid-State Electronics 103 (2015) 122–126

Contents lists available at ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

Design, fabrication and test of novel LDMOS-SCR for improving holding voltage

Liu Yang, Yang Wang, Acheng Zhou, Xiangliang Jin *

Faculty of Materials, Optoelectronics and Physics, Xiangtan University, Xiangtan 411105, China
Hunan Engineering Laboratory for Microelectronics, Optoelectronics and System on a Chip, Xiangtan 411105, China

ARTICLE INFO

Article history:
Received 8 April 2014
Received in revised form 9 August 2014
Accepted 15 August 2014
Available online 10 September 2014

The review of this paper was arranged by Prof. S. Cristoloveanu

Keywords:
LDMOS-SCR
TCAD
ESD
TLP

ABSTRACT

A novel structure, which is achieved by inserting P+ slots into the polygate of traditional LDMOS-SCR, has been designed to improve the holding voltage. The proposed structure called GateDot was fabricated in 0.5 μm 18 V CDMOS process. In this study, comparative analysis is carried out to make detailed comparisons between conventional LDMOS-SCR and the new proposed structure. GateDot not only maintains superiorities of low trigger voltage and strong capability of shunting ESD current in conventional LDMOS-SCR structure, but also increases the holding voltage greatly. To verify its advantages, theoretical analysis and TCAD device simulations were provided during the course of research. TLP (Transmission Line Pulse) test has been done and the results show that the holding voltage can effectively increase from 7.00 V to 10.17 V, 45.29% increment compared to traditional LDMOS-SCR, which is highly appeal to the simulation results.

© 2014 Elsevier Ltd. All rights reserved.

1. Introduction

With the rapidly increasing demands on high voltage (HV) technology applied in power ICs, electro-static discharge (ESD) protection has become a major challenge and attracts much more attention recently [1–3]. Lateral double-diffusion MOS (LDMOS) has been used widely as a common ESD protection device due to its high operating voltage and small leakage current [4–6]. Furthermore, the LDMOS has a strong "snapback" (low holding voltage at high trigger voltage). Lower holding voltage contributes to higher ESD protection levels since it makes the LDMOS a lower power dissipation device and thus protects the device from self-heating effect [7]. However, the LDMOS also has inevitable shortcomings, such as low ESD discharge capability per unit length and non-uniform current distribution in multi-finger devices [8]. Silicon-controlled rectifiers (SCRs) known as thyristors are used extensively in power device applications because of their highest efficiency among all protection devices in terms of ESD performance per unit area [9,10]. Therefore, in order to get better ESD protection robustness and performance, a novel structure called LDMOS-SCR (SCR embedded LDMOS) has been presented in many papers [11–13]. LDMOS-SCR has greater capability of shunting ESD current than conventional LDMOS due to positive feedback of SCR. However, LDMOS-SCR has a relatively low holding voltage and a tendency of suffering from latch-up, especially when it is applied to power-rail ESD clamp [14].

In this work, a novel structure named GateDot was presented to compensate the holding voltage of LDMOS-SCR pulled down by parasitic SCR. The proposed layout technique, which will significantly improve the holding voltage, was designed by inserting P+ slots into the polygate of LDMOS-SCR. With high holding voltage, the structure is immune to latch-up issue. Besides, since it was a LDMOS-SCR in essence, the superiorities in low trigger voltage and strong shunting current capability was also reflected.

2. Device structure and operation mechanism

2.1. Structure description

GateDot 3D structure is shown in Fig. 1. What differs from traditional LDMOS-SCR is that GateDot has P+ slots in the polygate. In other words, it consists of two kinds of segments. One segment is traditional LDMOS-SCR illustrated in Fig. 2(a). And as shown in Fig. 2(b), another segment, which is called Dot in this paper, is modified from LDMOS-SCR by inserting P+ slots into polygate. Equivalent circuits named SCR of the two segments each consist of a cross-coupled PNP bipolar transistor and NPN bipolar transistor in

* Corresponding author at: Faculty of Materials, Optoelectronics and Physics, Xiangtan University, Xiangtan 411105, China. Tel./fax: +86 731 5829 2468.
E-mail address: jinxl@xtu.edu.cn (X. Jin).

http://dx.doi.org/10.1016/j.sse.2014.08.007
0038-1101/© 2014 Elsevier Ltd. All rights reserved.

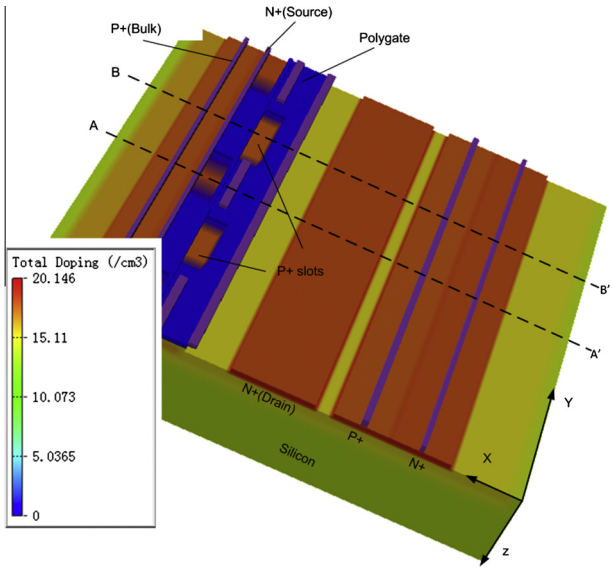

Fig. 1. ESD protection device GateDot 3D structure.

Fig. 2(a) and (b), which make the segments obtaining main paths to discharge ESD current. The positive-feedback mechanism of the embedded SCR makes devices high robustness against ESD stress.

2.2. Increment of holding voltage in Dot structure

For the bipolar transistor, its current amplification factor α can be expressed as:

$$\alpha = \gamma \times \beta^* \times \alpha^* \times M \tag{1}$$

where γ is the emitter injection efficiency, β^* is the base transmission factor, α^* is the collector multiplication factor and M is the avalanche multiplication factor. It is obvious that the bipolar transistor current amplification factor α is proportional to the emitter injection efficiency γ when other parameters are fixed. Eq. (2) describes how the emitter injection efficiency γ is affected by other physical parameters.

$$\gamma = \frac{1}{1 + \frac{N_B}{N_E} \cdot \frac{D_E}{D_B} \cdot \frac{X_B}{X_E}} \tag{2}$$

In Eq. (2), N_B, N_E, D_E, D_B, X_B and X_E represent the base doping concentration, the emitter doping concentration, the base minority carrier diffusion coefficient, the emitter minority carrier diffusion coefficient, the base effective width and the emitter effective width respectively. As Eq. (2) indicates, the emitter injection efficiency γ will be boost by increasing the base effective width X_B.

In this study, it is very significant for the Dot segment when P+ slots were inserted into the polygate, which increases the area of P+ diffusion. In general, the area of the effective base strongly depends on the size of the P+ diffusion for NPN transistor. So X_B becomes larger as the effective base area increases while other parameters keep the same. Therefore, the bipolar transistor current amplification factor α becomes lower than the LDMOS-SCR segment as the emitter injection efficiency γ of Dot segment becomes lower than before. When discharging the same amount of current as LDMOS-SCR segment does after the transistor being turned on, the Dot segment needs much higher voltage to maintain the feedback current of SCR. Therefore, the holding voltage of the Dot segment increases dramatically.

2.3. Characteristics of GateDot

The analysis of GateDot, which is composed of Dot segments and LDMOS-SCR segments in this work, is carried out as follows. Both the LDMOS-SCR segments and the Dot segments generate avalanche current due to the avalanche breakdown before the GateDot triggers on. Once the LDMOS-SCR segments turns on, they will promote the whole device triggering on. Because of the trigger of the LDMOS-SCR segments, each R_{on} of the LDMOS-SCR segments

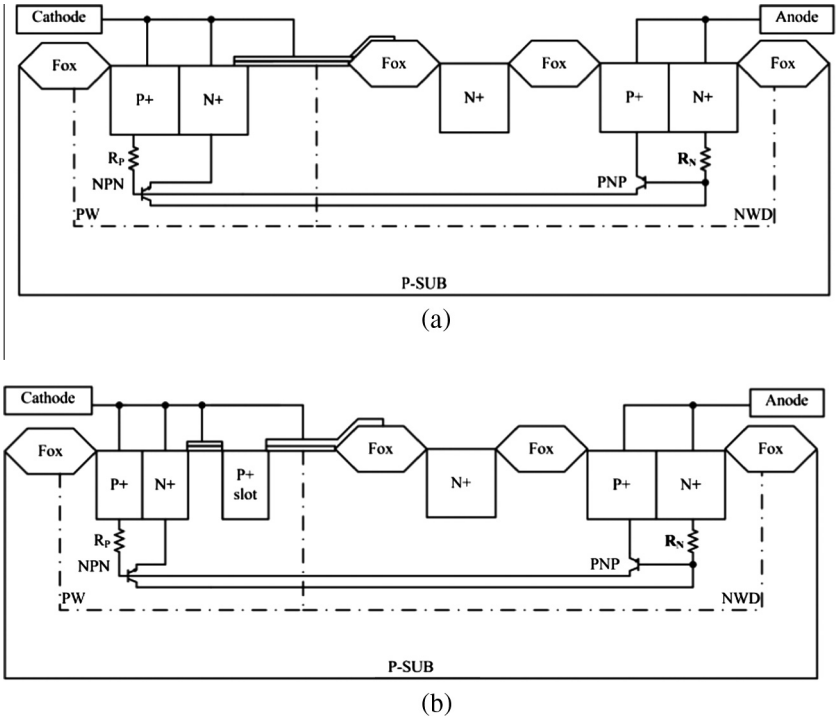

Fig. 2. Cross-sectional views and equivalent circuits of (a) the LDMOS-SCR segment from the section of dashed line A–A′ in Fig. 1, and (b) Dot segment from the section of dashed line B–B′ in Fig. 1.

Download English Version:

https://daneshyari.com/en/article/747875

Download Persian Version:

https://daneshyari.com/article/747875

Daneshyari.com