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Polycrystalline silicon thin-film transistors fabricated by Joule-heating-induced crystallization

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ABSTRACT

Joule-heating-induced crystallization (JIC) of amorphous silicon (a-Si) films is carried out by applying an electric pulse to a conductive layer located beneath or above the films. Crystallization occurs across the whole substrate surface within few tens of microseconds. Arc instability, however, is observed during crystallization, and is attributed to dielectric breakdown in the conductor/insulator/transformed polycrystalline silicon (poly-Si) sandwich structures at high temperatures during electrical pulsing for crystallization. In this study, we devised a method for the crystallization of a-Si films while preventing arc generation; this method consisted of pre-patterning an a-Si active layer into islands and then depositing a gate oxide and gate electrode. Electric pulsing was then applied to the gate electrode formed using a Mo layer. The Mo layer was used as a Joule-heat source for the crystallization of pre-patterned active islands of a-Si films. JIC-processed poly-Si thin-film transistors (TFTs) were fabricated successfully, and the proposed method was found to be compatible with the standard processing of coplanar top-gate poly-Si TFTs.

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1. Introduction

Low-temperature polycrystalline silicon (LTPS) is a crucial active layer material for polycrystalline silicon thin-film transistors (poly-Si TFTs) on thermally susceptible glass substrates. LTPS-TFT backplanes are required for fabricating flat panel displays such as active-matrix liquid displays and active-matrix organic light-emitting displays (AMOLEDs). LTPS-TFT backplanes are strongly preferred to amorphous silicon (a-Si)-TFT ones since several devices, AMOLEDs in particular, operate in a current-driven mode [1]. Methods used for forming LTPS include solid-phase crystallization (SPC) [2], metal-induced crystallization (MIC) [3], and excimer laser crystallization (ELC) [4].

Sameshima et al. were the first to report Joule heating crystallization carried out using Cr strips as heating sources in order to rapidly crystallize silicon films [5]. They crystallized 50-nm-thick a-Si films via 200-nm-thick SiO_2 intermediate layers by applying an electric field to Cr strips with a power density of $\sim 10^5$ W/cm^2. Extending this concept further, we have developed a crystallization method for a-Si films called Joule-heating-induced crystallization (JIC) [6–9]. In this method, an electric field is applied to a conductive layer above or beneath a-Si films to induce Joule heating that in turn leads to crystallization of the films. The film temperature in this method is more uniform than that achieved using other conventional heating methods since the Joule heat is generated uniformly throughout the conductive layer. The optimum processing windows for the JIC process strongly depend on the power density (W/cm^2) and pulsing time applied during the process. These process parameters determine the heating rate as well as the depth of thermal penetration from the Joule-heat source. Several instabilities have been observed when these parameters do not lie in a stable processing window, including glass bending, glass breaking, and the peeling off of thin film layers. Thus, complete crystallization over the whole substrate area without any instability can only be achieved by applying an electric field of a suitable magnitude to a conductive layer for a very short time (typically, <1 ms). However, the generation of an intense arc has been observed during the application of an electric field under suitable processing conditions to induce complete crystallization without any of the abovementioned instabilities. In this study, we devised a method for preventing arc generation during the JIC process. Further, we successfully fabricated poly-Si TFTs by using JIC samples prepared in this study.

2. Experimental

A schematic cross section of the JIC samples used in this study is shown in Fig. 1a. The process flow for fabricating JIC poly-Si TFTs is

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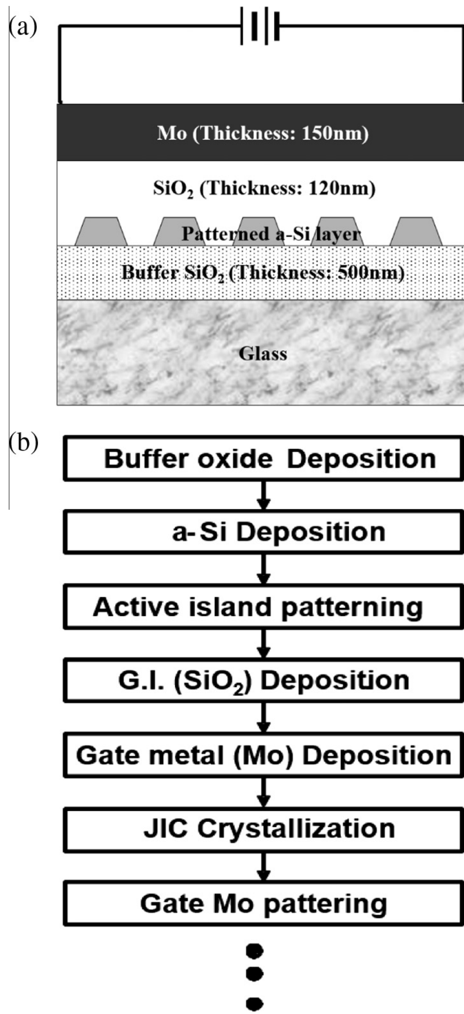

Fig. 1. (a) Schematic cross-section of a JIC sample in which silicon films are electrically floated. (b) Electric potential of conductor (solid line) and silicon (dotted line) as a function of distance at high temperatures, where sufficient mobile charge carriers are generated for conduction.

illustrated in Fig. 1b. The substrates used in this study were Corning 7059 glasses with dimensions of $20 \times 30 \times 0.7\ mm^3$. First, plasma-enhanced chemical vapor deposition (PECVD) was used to form a SiO_2 buffer layer (the first dielectric layer) with a thickness of 500 nm on a glass substrate. Moreover, the PECVD method resulted in a 50-nm-thick a-Si thin film being deposited on the first dielectric layer. This a-Si film was patterned and dry-etched to form active islands before the deposition of a 120-nm-thick oxide as a gate insulator. A 150-nm-thick Mo layer was then deposited by sputtering to form the gate metal. This Mo layer was also used as a Joule-heat source for the crystallization of the a-Si films. An electric field was applied to a Mo film with dimensions of $20 \times 20\ mm^2$ for 11 μs in order to crystallize the pre-patterned a-Si islands. Thereafter, the Mo layer was patterned and wet-etched to form a gate electrode. Self-aligned ion implantation was conducted to form a source/drain by using 30 keV B^+ ions at a dose of $1 \times 10^{15}/cm^2$. Activation annealing was performed at 450 °C for 1 h by using a tube furnace in nitrogen ambient.

3. Results and discussion

We have previously reported the mechanism of arc generation in JIC samples during electric-field application [10]. The structure of the JIC sample used in this study was a conductor/SiO_2/a-Si/SiO_2/glass sandwich structure, as shown in Fig. 2a. During electrical pulsing, the temperature of silicon films may approach or surpass their melting point, depending on the processing parameters such as power density and pulsing time. a-Si is transformed into poly-Si at temperatures near the melting point of silicon where it becomes a conductor. At this point, the system of interest attains a conductor/SiO_2/Si-conductor capacitor structure in which vertical generation of sparks may occur when the potential difference (ΔV, as indicated in Fig. 2b) between the conductor and silicon exceeds the dielectric breakdown voltage of the SiO_2 insulator. This, in turn, is followed by the generation of an intense arc because of an open circuit that forms under the applied electric field. In order to avoid this phenomenon, methods need to be devised to facilitate the preparation of a JIC sample in which equal potentials exist between the silicon and conductor. Fig. 2c shows the equivalent circuit for the structure shown in Fig. 2a. V_a–V_g respectively denotes the potential at each position of the conductor formed by the potential generated by the pulse power supply. The conductor has a constant resistance, and thus, it forms the potentials from V_a to V_g that decrease linearly. In the initial stage of voltage application, V'_a to V'_g respectively denote the potential at each position of the Si conductor formed by the potential because of a floating capacitor (C_a–C_g) formed by SiO_2 deposited between the insulator and silicon. In other words, $V_a = V'_a > V_b = V'_b > \cdots > V_g = V'_g$. If the current flowing because of the potential difference formed on the silicon thin film is large enough to charge the capacitor (C_a–C_g), the current flow would result in equivalent potentials from V'_a to V'_g owing to the fact that no external electric charges are being added, and C_a–C_g gets charged. When such a potential difference, i.e., V_a to V'_a or V_b to $V'_b \cdots V_g$ to V'_g, in the capacitor is larger than the breakdown voltage of the capacitor, dielectric breakdown occurs.

In order to prevent arc generation, the potential difference between the conductor and silicon should be smaller than the

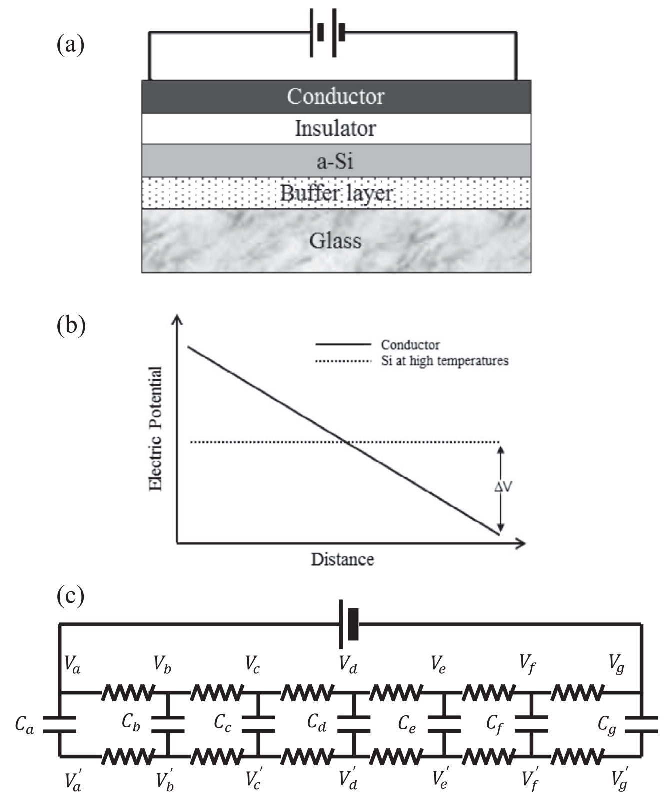

Fig. 2. (a) Schematic cross-section of a JIC sample used in this study. (b) Steps involved in fabrication of JIC poly-Si TFTs. (c) A diagram of an equivalent circuit.

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