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Modeling and simulation of Double Gate Junctionless Transistor considering fringing field effects

Vandana Kumari [a,d], Neel Modi [b], Manoj Saxena [c], Mridula Gupta [a,*]

[a] Semiconductor Device Research Laboratory, Department of Electronic Science, University of Delhi, South Campus, New Delhi, India
[b] Electronics and Communication Engineering, Sardar Vallabhbhai National Institute of Technology (SVNIT), Surat, India
[c] Department of Electronics, Deen Dayal Upadhyaya College, University of Delhi, India
[d] Department of Electronics, Maharaja Agrasen College, University of Delhi, New Delhi, India

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ABSTRACT

In the present work, the performance of DG-JL transistor has been analysed using analytical modeling scheme as well as 3D device simulation technique. Thus an advance two dimensional analytical sub-threshold drain current model for Double Gate Junctionless (DG-JL) Transistor is presented in this work by considering the impact of fringing field from the gate to source/drain region using conformal mapping technique. The results obtained from proposed model have been verified with the ATLAS 3D device simulation software results. The relevant Short Channel Effect parameters like threshold voltage roll off, Drain Induced Barrier Lowering (DIBL) and Subthreshold Slope (S) are also evaluated using modeling scheme. In addition to this, the suitability of DG-JL Transistor for low voltage digital and analog applications has been investigated through exhaustive device simulation using ATLAS 3D device simulation software only. In essence, this work provides the dependencies of the device performance on the physical device parameters of DG-JL transistor for its assessment for better digital and analog operation.

1. Introduction

In order to improve the device performance, the channel length of the conventional MOSFET has been continuously scaled down. This will eventually causes severe Short Channel Effects (SCEs) like threshold voltage roll-off and Drain Induced Barrier Lowering (DIBL) [1]. Recently, a remarkably efficient device design i.e. Junctionless (JL) Transistor has been proposed and fabricated to overcome the insufficiency of conventional MOSFET due to aggressive scaling [2]. Moreover the fabrication process steps are also comparatively simpler for Junctionless (JL) Transistor [2]. As a result of similar doping profile of source/drain as well as the channel of JL transistor, the behavior of the device can easily be described by resistor in which the gate controls the current density and hence current flow inside the channel [3]. The device offers less resistance (i.e. turned on), when the external applied gate voltage is equal to flat band voltage. In addition to this, compared to conventional MOSFET, the doping level of JL transistor is significantly high i.e. 10^{18} cm^{-3} to 10^{19} cm^{-3}. The advantages of JL transistor also includes: (1) lower leakage current, (2) high I_{on}/I_{off} ratio, (3) lesser sub-threshold slope and variability. However, it is difficult to fully deplete the channel region of JL transistor by utilizing the single gate control [4], [5]. Thus the main concern of the present work is devoted towards the Double Gate architecture i.e. Double Gate Junctionless (DG-JL) Transistor.

Various models have been reported in the literature regarding the analytical modeling of double gate JL transistor [6–12]. But these models work under the approximation that the impact of source/drain region length on the channel potential is negligible (i.e. the source drain regions are un-depleted). In 2013 Gnudi et al. [13] reported semi-analytical model for Double Gate Junctionless Transistor with depleted source and drain region. In this study, gate fringing field effect was ignored to calculate the potential inside the source/drain region which may lead to inaccurate results as channel length decreases. In addition, parabolic potential profile is assumed to calculate the potential inside the channel region. In 2013, Holij et al. presented an analytical model using Schwarz–Christoffel transformation to calculate the potential inside the channel [14]. Another charge based model for DG-JL transistor has also been reported recently using Schwarz–Christoffel transformation [7]. Thus there is need of analytical model for DG-JL Transistor which accounts for depleted source and drain region in order to accurately estimate the impact of S/D regions length on device performance under gate fringing field.

* Corresponding author.
E-mail addresses: vandanakumari511@gmail.com (V. Kumari), neelmodi92@gmail.com (N. Modi), saxena_manoj77@yahoo.co.in (M. Saxena), mridula@south.du.ac.in (M. Gupta).

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In the present work, sub-threshold drain current model of DG-JL Transistor has been presented using conformal mapping technique. In this modeling scheme source and drain regions are considered as fully depleted (such that the length of the source/drain region is taken smaller than the depletion width in the S/D region) in the sub-threshold region. Thus it is assumed that the potential inside the source/drain region varies linearly along the length of S/D region. The impact of spacer layer permittivity k on the performance of DG-JL transistor has also been accounted in this work using analytical model. Thus the complete work is divided into two parts: (1) In first part i.e. Sections 1 and 2, analytical model of DG-JL transistor has been presented and the obtained results are compared with the simulated results from ATLAS 3D device simulation respectively. (2) In later part i.e. Sections 3 and 4, the performance of DG-JL transistor have been analyzed for analog (amplifier) and digital (CMOS inverter) performance respectively by making parametric variations such as channel doping, length, spacer permittivity and source drain length. Thus the results presented in Sections 3 and 4 are obtained using ATLAS 3D device and circuit simulation only.

Validation of analytical results was made by using ATLAS 3D device simulation results [15]. The performance comparison presented in Sections 3 and 4 are also based on the results obtained from TCAD simulation. The numerical simulations are performed using models such as transverse field dependent, temperature dependent mobility model and Shockley and Read Hall recombination model. Hydrodynamic transport model has been used along with the band gap narrowing model due to the high channel doping. Fermi Dirac distribution has been used in the present analysis.

2. Analytical modeling

The schematic cross section view of DG JL transistor is shown in Fig. 1a. L is the length of the channel, W is the width of the device. The device architecture is divided into three different regions: channel, source and drain regions. For channel region (Region II), potential is found out by using Evanescent Mode Analysis (EMA) technique [16,17]. For source and drain regions i.e. region I and III, it is assumed that the potential is a linear function of the length of the source/drain region. The potential in the S/D regions is found out by using conformal mapping technique [18,19].

2.1. Band gap narrowing

Due to the reduction in conduction band level at higher channel doping, the effective band gap decreases which is modeled as [15]:

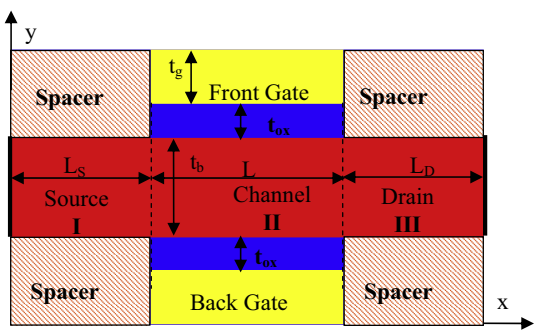

Fig. 1a. Schematic cross sectional view of Double Gate Junctionless (DG-JL) Transistor. Regions I and III are S/D regions; L_S and L_D are the length of source/drain regions, L is the channel length i.e. the length under the gate control, t_b is the thickness of silicon body and t_{ox} is upper and lower gate oxide thickness, t_g is the thickness of the upper and lower gate.

$$\Delta E_g = BGN.E\left[\ln\frac{N_b}{BGN.N} + \left[\ln\frac{N_b}{BGN.N} + BGN.C\right]^{0.5}\right] \tag{1a}$$

BGN.E, BGN.N and BGN.C are material constants i.e. 9×10^{-3} V, 1×10^{17} cm^{-3} and 0.5 respectively [15]. Subsequently, intrinsic carrier concentration (n_{ieff}) [20] as well as the electron affinity (χ_{eff}) of doped silicon also modified and can be modeled as:

$$n_{ieff} = \sqrt{n_i^2 \exp\left(\frac{\Delta E_g}{k_b T}\right)} \tag{1b}$$

$$\chi_{eff} = \chi + \Delta E_g 0.5 \tag{1c}$$

n_i and χ are the intrinsic concentration and electron affinity before employing band gap narrowing model.

2.2. Modeling in channel region (Region II)

The mobile charge carriers have been neglected in the channel region since only sub-threshold region is considered here. Thus the potential in the channel region (i.e. for region I) is formulated by using 2-D Poisson's equation which is given as:

$$\frac{\partial^2\psi_2(x,y)}{\partial x^2} + \frac{\partial^2\psi_2(x,y)}{\partial y^2} = \frac{-qN_b}{\varepsilon_{si}} \tag{2a}$$

where $0 < y < t_b$ and $L_S < x < L + L_s$.

N_b is the doping concentration of channel and S/D region. ε_{si} is permittivity of silicon channel. The potential ψ_2 (x,y) is the complete two dimensional potential in the channel region and it is calculated by dividing it into 1-D potential ψ_{12} (y) (which is found out by solving 1D Poisson's equation) and 2-D ψ_{22} (x,y) (which is found out by solving 2D Laplace equation) as:

$$\psi_2(x,y) = \psi_{12}(x) + \psi_{22}(x,y) \tag{2b}$$

The corresponding 1D Poisson's equation is given as:

$$\frac{\partial^2\psi_{12}(y)}{\partial y^2} = \frac{-qN_b}{\varepsilon_{si}} \tag{2c}$$

The corresponding 2D Laplace equation is given as:

$$\frac{\partial^2\psi_{22}(x,y)}{\partial x^2} + \frac{\partial^2\psi_{22}(x,y)}{\partial y^2} = 0 \tag{2d}$$

The solution of 1D Poisson's equation (i.e. 1D potential in the channel region) is given as:

$$\psi_{12}(y) = \frac{-qN_b}{2\varepsilon_{si}}y^2 + c_1 y + c_2 \tag{3a}$$

The boundary conditions arising from the continuity of potential and electric field at the interface of different boundaries [21] are used to calculate one dimensional constants (i.e. c_1 and c_2) and are given as:

$$c_1 = \frac{\frac{qN_b t_b^2}{2\varepsilon_{si}} + \frac{t_{ox} qN_b t_b}{\varepsilon_{ox}}}{t_b + \frac{2t_{ox}\varepsilon_{si}}{\varepsilon_{ox}}} \tag{3b}$$

$$c_2 = V_{gs} - \phi_{ms} + \frac{\frac{qN_b t_b^2 t_{ox}}{2\varepsilon_{ox}} + \frac{t_{ox}^2 qN_b t_b \varepsilon_{si}}{\varepsilon_{ox}^2}}{t_b + \frac{2t_{ox}\varepsilon_{si}}{\varepsilon_{ox}}} \tag{3c}$$

where ϕ_{ms} is flat-band voltage for both front and back gate.

The solution of the 2D Laplace equation (i.e. Eq. (2d)) is given as [12]:

$$\psi_{22}(x,y) = \{C\sinh[\gamma(L_S + L - x)] + D\sinh[\gamma(L_S - x)]\}\sin(\gamma_n y) \tag{4a}$$

where