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Pulse-width-independent low power programmable low temperature poly-Si thin-film transistor shift register

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ABSTRACT

This paper demonstrates a low power programmable pulse width LTPS TFT shift register which achieves the constant power consumption over various pulse widths with the smaller number of TFTs compared to the previous programmable shift register. The proposed shift register consists of nine *n*-channel LTPS TFTs and one coupling capacitor. By eliminating the shoot-through current path in a NOT–AND logic, the simulation ensures that the proposed structure reduces the power consumption significantly by 60.5% for two line pulse width and by 88.6% for ten line pulse width from the previous programmable pulse width shift register. The power consumption of 12 shift registers is measured at 0.235 mW, independently of programmed pulse widths.

1. Introduction

Active matrix flat panel displays such as active matrix liquid crystal displays and active matrix organic light emitting diode (AMOLED) displays have occupied most of display markets due to their advancement in size, resolution, frame rate [1–5]. However, these high performances lead to large capacitive and resistive line load as well as small line time, which cause the insufficient charging time for pixel electrodes. A pre-charging scheme can secure enough charging time by utilizing multiple line times for one pixel. To support the pre-charging method, shift registers need to generate output pulses with some overlap intervals [6–8]. Most of thin film transistor (TFT) overlap shift registers employ multi-phase clock signals which are used to drive the output nodes directly. Consequently, the output pulse width is programmed in accordance to the clock pulse width. On the other hand, a programmable pulse width low temperature poly-Si (LTPS) TFT shift registers have been proposed to adjust the output pulse width only by changing a start pulse width without any additional clock signals and circuit modification [9]. The programmable shift register enables multi-rate panels of low fabrication cost which can be employed at various frame rate applications such as 60 Hz, 120 Hz, and 240 Hz, by means of the pre-charging scheme of variable overlap intervals. Whereas, conventional shift registers cannot be applied to multi-rate displays since the number of clock signals and interconnections between shift register cells must be modified according to target pulse widths. In addition, the programmable shift register can be applied to make long control signals for the pixel compensation circuits of AMOLED displays with clock signals used for the scanning pulse generation [10,11].

This paper presents a programmable pulse width LTPS TFT shift register that achieves the lower constant power consumption regardless of pulse width along with the reduced number of TFTs compared to a previous programmable shift register [9].

2. Proposed programmable shift register circuit

Fig. 1(a) shows the schematic of a proposed programmable pulse width shift register which consists of nine *n*-channel TFTs (N1–N9) and one boosting capacitor (C1). A NOT–AND logic generates a $B[n]$ signal which is a gated clock signal with $V_g[n-1]$ and CLK1. Fig. 1(b) describes the timing diagram of the proposed shift register when the output pulse width is equal to four line times. Two clock signals of fixed frequency and duty ratio (CLK1, CLK2) are utilized, regardless of output pulse widths, for whole gate driver circuitries. The pulse widths of CLK1 and CLK2 are set to one line time and CLK2 is out of phase with CLK1. When CLK1 is provided to one stage, CLK2 is connected to a next stage.

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The key differences between proposed and previous schemes [9] are $Q[n]$ discharging path and NOT–AND circuit. In the previous programmable shift register depicted in Fig. 2, the $Q[n]$-node is charged and discharged through two separate TFTs (T1, T12). The gate signal of T1 is generated as the gated clock ($A[n]$) by means of two TFTs (T10, T11), which is the output of an AND operation of $V_g[n-1]$ and CLK1. As a consequence, T1 is used only to charge the $Q[n]$-node with $V_g[n-1]$. T12, that is controlled by another gated clock signal ($B[n]$), is added to support the discharging path of a $Q[n]$-node. However, the proposed one drives the $Q[n]$-node via only one TFT (M1) directly connected to CLK1, where three TFTs of T10, T11, and T12 as well as the connection to CLK2 are eliminated. Because one clock signal drives only one TFT every other shift register, the capacitive loads of clock signals are reduced, leading to the lower power consumption. With respect to a NOT–AND circuit, while the previous circuit includes the shoot-through current path between VDD and VSS due to the diode-connection load of a first stage inverter [12], the proposed structure adopts the $Q_b[n-1]$ signal from a previous shift register stage to turn the load TFT (M2) off completely during the high interval of $V_g[n-1]$. In the previous NOT–AND circuit, as T2 is always on-state, the shoot-through current from VDD to VSS flows through T2 and T3 as shown in Fig. 3(a). Consequently, the longer pulse width of $V_g[n-1]$ consumes the more power. On the contrary, because the proposed scheme removes the shoot-through current path by using the $Q_b[n-1]$ signal which is an inverted one of $V_g[n-1]$ as illustrated in Fig. 3(b) and (c), the further power consumption reduction can be achieved. In addition, the constant power consumption feature is accomplished independently of output pulse widths. The delay between $Q_b[n-1]$ and $V_g[n-1]$ can cause the small amount of the shoot-through current in the proposed NOT–AND circuit. However, the current is proportional to the delay interval but not to the pulse width, where the pulse-width-independency is still guaranteed.

Similarly to the previous programmable shift register, the operations of the proposed circuit are divided into four periods such as Q-generation, Q-boosting, one-line delay, and pull-down. Each operation is explained in more detail as follows.

(1) *Q-generation:* $V_g[n-1]$ charges a $Q[n]$-node into high voltage through M1 turned on by CLK1, one line time after the rising transition of $V_g[n-1]$. A $B[n]$-node is pulled down to VSS via M5 due to the high voltage level of $V_g[n-1]$. Since M6 is turned off by $B[n]$ and M7 is turned on by $Q[n]$, $Q_b[n]$ is set to VSS through M7 and $V_g[n]$ is driven up by VDD through M8.

(2) *Q-boosting:* Since the $Q[n]$-node voltage in the Q-generation period is not enough high to achieve the high level of $V_g[n]$ at VDD, the next stage output ($V_g[n+1]$) is connected to $Q[n]$ through a coupling capacitor (C1) and the high voltage level of a $Q[n]$-node is boosted further by capacitive coupling at the rising transition of $V_g[n+1]$. Thus, $V_g[n]$ can be completely charged up to VDD.

(3) *One-line delay:* After $V_g[n-1]$ becomes VSS, $V_g[n]$ has to maintain high voltage for one more line time to keep the pulse width of $V_g[n]$ equal to that of $V_g[n-1]$. While M1 is turned off by the low voltage of CLK1, $Q[n]$ remains at high voltage. In addition, a $B[n]$-node is settled at VSS due to the low voltage of CLK1 and $V_g[n]$ continues to be driven by VDD for one more line time.

(4) *Pull-down:* Since M1 becomes turned on at the high voltage of CLK1, $Q[n]$-node is discharged by the low voltage of $V_g[n-1]$, which causes M8 to be turned off. On the other hand, a $Q_b[n]$-node is charged up to VDD through M6 by the high voltage of $B[n]$ while M7 is turned off by the low voltage of $Q[n]$. As a consequence, $V_g[n]$ is pulled down to VSS through M9.

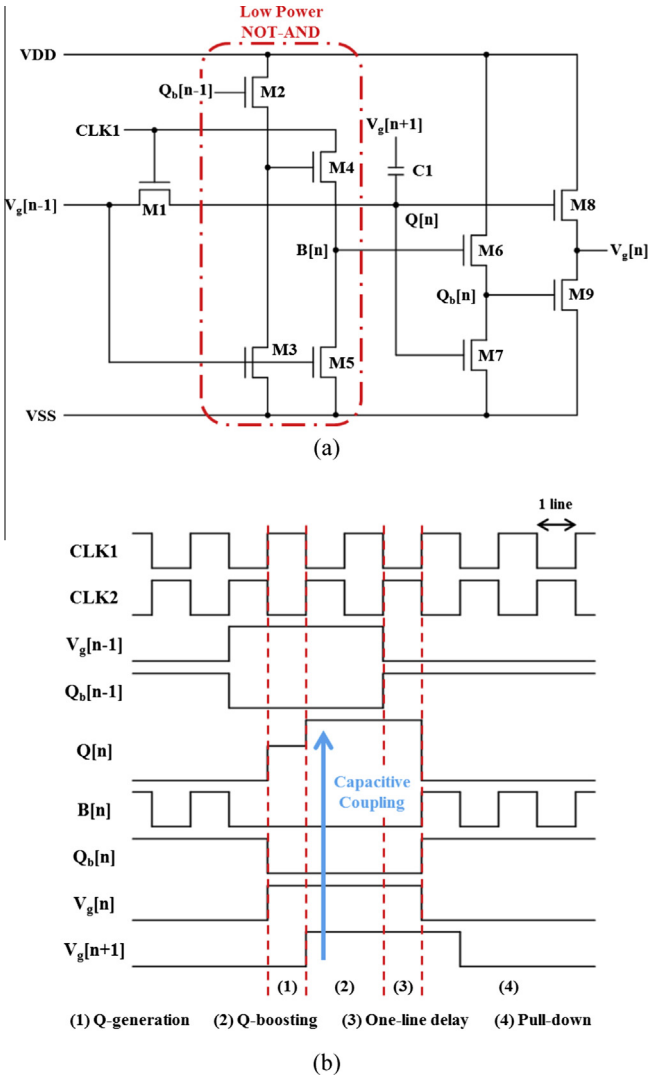

Fig. 1. Proposed programmable pulse width shift register (a) schematic and (b) timing diagram.

3. Measurement results

A programmable gate driver circuit of 12 shift registers was fabricated with n-channel LTPS TFTs of a lightly doped drain (LDD) and coplanar structure. The threshold voltage, mobility, and overlap capacitance of TFTs are 1.94 V, 37.907 cm^2/Vs, and 0.16 fF/μm. The metal–insulator–metal (MIM) structure is employed for a boosting capacitor with the unit capacitance of 0.08 fF/μm^2. The channel length is 5.5 μm and channel widths of TFTs are summarized in Table 1. The boosting capacitor C1 is 1 pF and VDD and VSS are set to be 20 V and −5 V. Fig. 4 presents the micrograph of a 12-stage proposed gate driver circuit.

The measured waveforms are shown in Fig. 5 for the pulse widths of two, four, six, eight, and ten line times where a line time and a clock frequency are set to 8 μs and 129.6 kHz, respectively. The measured power consumption is described in Table 2 according