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Technological development of high-*k* dielectric FinFETs for liquid environment

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ABSTRACT

This work presents the technological development and characterization of n-channel fully depleted high-k dielectric FinFETs (Fin Field Effect Transistor) for applications in a liquid environment. Herein, we provide a systematic approach based on Finite Element Analysis for a high-control fabrication process of vertical Si-fins on bulk and we provide many useful fabrication expedients. Metal gate FinFETs have been successfully electrically characterized, showing excellent subthreshold slope SS = 72 mV/dec and high $I_{on}/I_{off} \approx 10^6$ ratio, with power consumption of the order of tens of nW. The FinFETs have also been proved to correctly behave in a liquid environment. We also present the HfO_2 characterization towards full pH response sensing applications.

1. Introduction

Silicon Nanowires (SiNWs) are emerging as the next generation of label-free sensors for biochemicals and bio-entities [1,2], featuring better performances with respect to their planar counterparts, i.e., Ion-Sensitive Field Effect Transistors (ISFET) [3]. However, circuit integration and mass production are still a demanding challenge, partially because a great extent of the work related to SiNWs does not focus on the innovation of the device architecture, based on structure with rather large width and reduced thickness ($H_{SiNW}/W_{SiNW} < 1$, Fig. 1) [4–6]. Fabrication is usually limited to Silicon-On-Insulator (SOI) wafers and solutions are rarely proposed for development on bulk Si. Moreover, power consumption is barely taken into account and many proposed devices are biased at high voltages [4,5,7–9] or the use of a back-gate [8,10] is not confronted with the need for CMOS compatibility.

Herein, we propose the implementation of an *n-channel fully depleted FinFET on Si-bulk*, not yet specifically used for sensing applications. Such advanced architecture is recognized to be one of the best performing electronic components thanks to the excellent electrostatic control provided by the multi-gate structure. Advanced models accurately describe the channel potential in the case of fully depleted multi-gate devices [11,12]. In parallel, a pH dependent surface potential can be expressed as:

$$\Phi(\mathrm{pH}) = 2.3\frac{kT}{q}\frac{\beta}{\beta+1}(\mathrm{pH}_{pzc} - \mathrm{pH}), \quad (1)$$

where k is the Boltzmann constant, T is the temperature, q the charge, pH_{pzc} is the point zero of charge and β determines the final sensitivity related to surface reactions [3].

When both potentials contribute to the device drain current, I_d, they have to be coupled in a unique potential, according to the field directions and biasing potentials:

$$\Phi^*_{ch} = \Phi_{ch} + \Phi(\mathrm{pH}), \quad (2)$$

where Φ^*_{ch} is the new FET channel potential, resulting from the combination of the initial FET channel potential and the potential induced by ionic charges or any other bio-entities.

The intrinsic sensitivity of a FET sensor is equivalent to the threshold voltage variation ΔV_{th} induced by the specific adsorption of positive or negative charge on the device's active surface. The maximum shift of the surface potential due to a change in pH is given by the Nernst limit of 59.5 mV/pH. In this context, high-*k* material such Al_2O_3 and HfO_2 have been demonstrated to be highly pH sensitive [13], reaching ΔV_{th} close to the Nernst limit.

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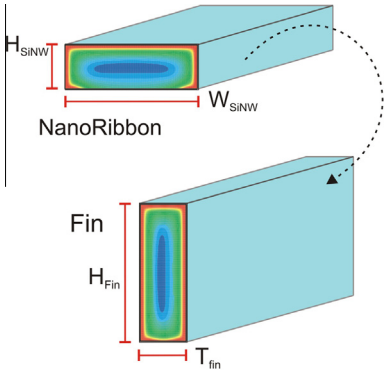

Fig. 1. NanoRibbon, as mostly used in sensing applications, and vertical FinFET as proposed in the presented work.

A readout sensitivity can also be defined if, instead of looking at the ΔV_{th}, a drain current variation ΔI_d is observed in a sensing event. For kinetic studies of fast bio-reactions, the sensing event cannot be observed in steady-state, as for the threshold voltage, thus the ΔI_d becomes very important. Additionally, a complete reference electrode voltage sweep could entail hysteretic behavior and ΔV_{th} could be difficult to be distinguished from such effect. The total $\Delta I_d/I_d$ results then from two contributions: the threshold voltage shift ΔV_{th} and the transistor subthreshold slope SS. Fig. 2 shows the two contributions with the threshold shift on the horizontal axis and the final ΔI_d on the vertical axis, which both ΔV_{th} and SS contribute to.

In this perspective, the design and the fabrication of performing transistors become a requirement for enhanced sensors and, mostly, for future scaling and advanced read-out circuits. For such reason we propose the FinFET architecture as both sensing and electronic unit, towards a low power sensing integrated circuit.

Fig. 2 also compares the simulated $I_d(V_g)$ of a NanoRibbon with respect to a FinFET when its length it is reduced from 2 μm to 200 nm: while the SS of the ribbon becomes less steep, no degradation occurs for the FinFET. To conclude, the presented work will provide an overall investigation on the key parameters for a successful fabrication of sub 20 nm liquid gate FinFETs on Si-bulk towards advanced sensing applications. On the other hand, we will characterize and optimize HfO_2 to guarantee the maximum intrinsic sensitivity.

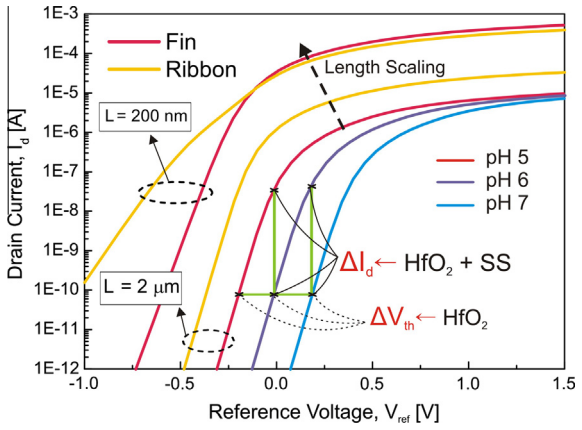

Fig. 2. A 3D FEA simulation shows the transfer characteristic $I_d(V_{ref})$ degradation when the length of a NanoRibbon device is scaled from 2 μm to 200 nm. No degradation occurs for the Fin ($T_{Fin} = H_{Rib} = 50$ nm and $W_{Rib} = H_{Fin} = 150$ nm); the threshold voltage shift and the output current variation upon a sensing event are underlined.

2. High-k dielectric characterization

P-type wafers with 10 nm HfO_2 deposited by ALD (Atomic Layer Deposition) were characterized, focusing the attention on different annealing processes. Capacitance–voltage measurements were performed at 1 MHz with the HP4248A capacitance meter at different voltage amplitude sweeps and the leakage current measurements by the 4156A precision semiconductor parameter analyzer connected to the low-leakage switching matrix B2200A. All measurements were performed in a light-proof, electrically shielded cascade probe station (Cascade Microtech Inc.).

Fig. 3 shows the high frequency capacitance obtained by sweeping the gate voltage from −2 V to 2 V and vice-versa. Both wafers treated with annealing process (500 °C for 1 h and 500 °C for 3 h) showed worst results in terms of accumulation capacitance and hysteresis compared to the not annealed wafer. The measured accumulation capacitance (C extrapolated at −4 V) for the not annealed devices was 140 pF, corresponding to a $\varepsilon_{ox} \approx 14.37$. With the 1 h annealing process the results were $C = 111.2$ pF and $\varepsilon_{ox} \approx 11.42$, while extending the annealing to 3 h the results were $C = 117.7$ pF and $\varepsilon_{ox} \approx 12.09$. As can be seen from Fig. 4, the annealing process clearly reduces the break-down voltage of the MOS capacitors. However, the gate current remains below 1 pA. The worsening of the C–V and I–V characteristics can be explained by the deterioration of the oxide after the annealing process due to the formation of an Hf-silicate at the silicon interface combined with a high number of interface traps typical of high-k material [14,15]. In order to limit this degradation effect the annealing should be limited to short time if it is needed after metallization (450 °C for 15 min), otherwise should be avoided. The final temperature parameters were 200 °C for the deposition chamber, 80 °C for the source of first precursor TEMAH and room temperature for second precursor H_2O.

Fig. 5 highlights that the increase of the hysteresis was caused only by the shift of the down sweep curve (from inversion to accumulation regime). This phenomenon of flat band voltage shift is the evidence of the presence of trapped charges of negative electronic nature. Indeed, when the voltage sweep was started from the accumulation the electrons trapped were released and there was no significant shift in flat band voltage. It has been noted that this behavior is more evident in wafers processed with annealing. By direct inspection of the results reported in Fig. 2 we note that the direction of the hysteresis is the same in all curves and it is consistent with electron trapping at the silicon-oxide interface. The degradation of the bulk oxide and interface due to the annealing process can explain the larger amount of trapped charges and consequently the increase of the hysteresis in wafers without annealing with respect to the not annealed wafer. The behavior

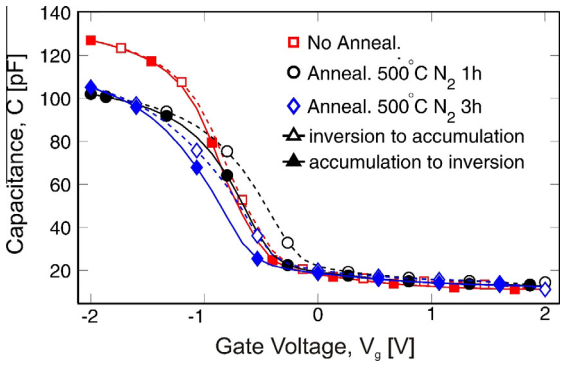

Fig. 3. C–V_g characteristics show the hysteresis of MOS (Al–HfO_2–Si) capacitors with and without annealing in N_2 ambient at 500 °C for 1 h and 3 h, with V_g sweep from −2 V to 2 V and backward.