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Strain effects on *n*-InGaAs heterostructure-on-insulator made by direct wafer bonding

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ABSTRACT

We have investigated the strain effects on the effective channel mobility of InGaAs pseudo (Ψ) *n*-MOSFETs by means of mechanical beam bending technique. For this goal, III–V heterostructures were grown on InP and transferred onto Si by direct wafer bonding. We show that an increase in electron mobility of up to 70% can be achieved under tensile strain. Simulations of InGaAs band-structure parameters under strain suggest that in the present case mobility enhancement is due to an increase of the sheet carrier density rather than to a decrease of the effective mass.

1. Introduction

Because of their high electron mobility, III–V semiconductor compounds are possible candidates for replacing Si in future high performance MOSFETs. An important target for CMOS technology is indeed a high-mobility *p*-type channel that matches by a factor 3–5 the mobility of the *n*-channel. Strain engineering is one of the well-known options to boost mobility in Si and Ge, but also in future III–V channel MOSFETs [1]. Several studies of the effect of uniaxial strain on electron and hole mobilities in such devices have been reported, using either wafer-bending methods [2–4], source/drain (S/D) stressor [5] or stress liner technology [6]. Mobility enhancement by biaxial strain on $In_{0.53}Ga_{0.49}As$ MOSFETs, using a relaxed buffer substrate technology, has also been demonstrated [7,8]. Indeed in that case, stress is applied to the channel material via in situ lattice mismatch, which deforms the crystal structure and thus alters the band structure. The tensile or compressive strain induced in direct band-gap semiconductors shifts their conduction band and splits the valence band, lifting the degeneracy between heavy hole and light hole subbands. Within Drude's model for electrical conduction, the change in carrier mobility under strain relates therefore to the variation of the ratio of the effective scattering time τ_{eff} over the in-plane effective mass m^*.

Here we propose a simple and rapid method to investigate strain effects on the effective channel mobility of InGaAs by combining the use of pseudo (Ψ) *n*-MOSFET structures and the mechanical beam-bending technique. The III–V heterostructures grown on an InP substrate are transferred onto Si via direct wafer bonding. This simple method allows a faster turnover without the need for a full device process flow. It is shown that an enhancement of the electron mobility by about 70% can be achieved under tensile strain. This behaviour is explained by comparing our experimental results with simulations of the band structure of InGaAs under strain.

2. Experimental

2.1. Device fabrication

A stack of $In_{0.52}Al_{0.48}As$-$In_{0.53}Ga_{0.47}As$-$In_{0.52}Al_{0.48}As$ layers is grown by metalorganic vapor-phase epitaxy (MOVPE) on a semi-insulating 2″ InP(100) wafer. The $In_{0.53}Ga_{0.47}As$ layer is 25 nm thick with a top lattice-matched InAlAs layer of 0, 5 or 10 nm. A capping layer of 35 nm Al_2O_3 – the buried oxide (BOX) – is deposited by atomic layer deposition (ALD). This entire structure is then bonded onto a 4″ Si(100) wafer annealed at 250 °C for 10 min to form strong covalent bonds. After etching away the InP wafer and the InAlAs interlayer, the tungsten top metal electrodes, with mesa isolation, are defined by lithography and lift-off processes (Fig. 1). The reason for using bonded structures on Si is to take advantage of the simple Ψ-MOSFET architecture and to reach potentially higher (typically up to 0.5%) strain values than on InP wafers, which are too brittle for this purpose. The high quality of

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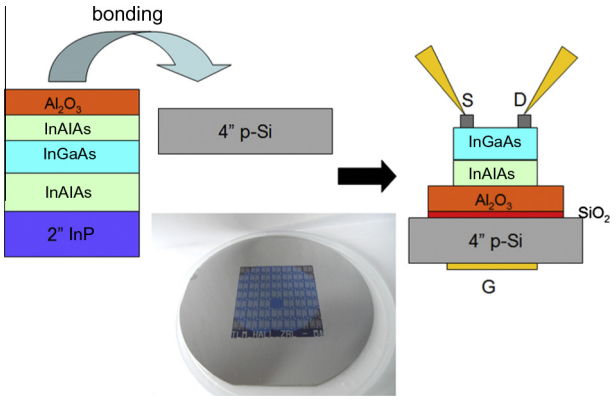

Fig. 1. Schematic of the III–V heterostructure growth on 2″ InP(100) wafer and direct wafer bonding process on 4″ Si(100) wafer for the fabrication of Ψ-MOSFET structures with etched lateral trenches for mesa isolation and patterned W contacts for source and drain. Electrical contact is made with probe needles. Included is a picture of the final bonded structures on the Si wafer.

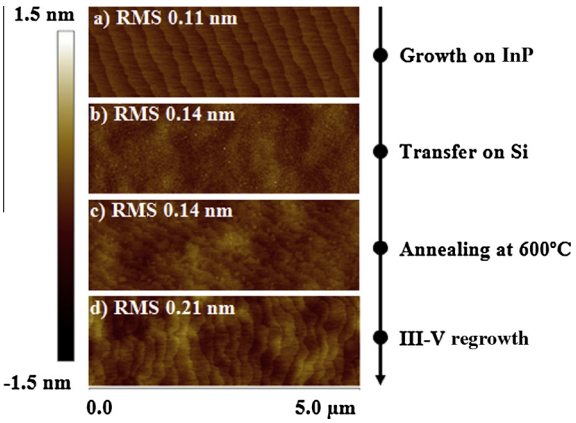

Fig. 3. AFM surface topography of InGaAs after several process steps, demonstrating low RMS roughness and thermal stability even after annealing at 600 °C and after regrowth.

the ultra-thin (fully depleted) InGaAs-on insulator layers obtained by direct wafer bonding has been investigated by spectroscopic ellipsometry, high-resolution X-ray diffraction (HR-XRD) and AFM imaging after various process steps [9]. It is observed that the thickness homogeneity, the high crystallinity (Fig. 2), and the low surface RMS roughness of InGaAs are kept after the transfer, after annealing at 600 °C, and even after regrowth of an additional 25 nm-thick InGaAs layer (Fig. 3). This confirms the excellent thermal stability of the stack under the bonding process. A picture of the final transferred structures is displayed in Fig. 1. Further details on the transfer of high-quality ultra-thin III–V heterostructures by direct wafer bonding and even hydrogen-induced thermal splitting can be found in [9,10].

2.2. Measurements

The transport measurements under uniaxial strain are performed with a mechanical beam bending apparatus (Fig. 4) using either a 3-point or 4-point bending configuration. The structured wafers are sliced into 25 mm × 4 mm pieces to fit into the setup, which was calibrated with commercial strain gauges.

Electrical contacts to the source S and drain D of the Ψ-MOSFET structures are done with needle probes. The backside of the Si substrate, covered with InGa eutectic, is used as gate electrode, G. Transfer length method (TLM) structures are also used to measure

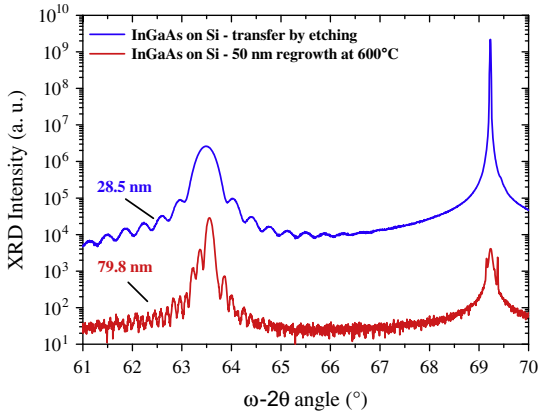

Fig. 2. High resolution XRD ω–2θ scans on the (004) reflection line of InGaAs after transfer and additional regrowth at 600 °C.

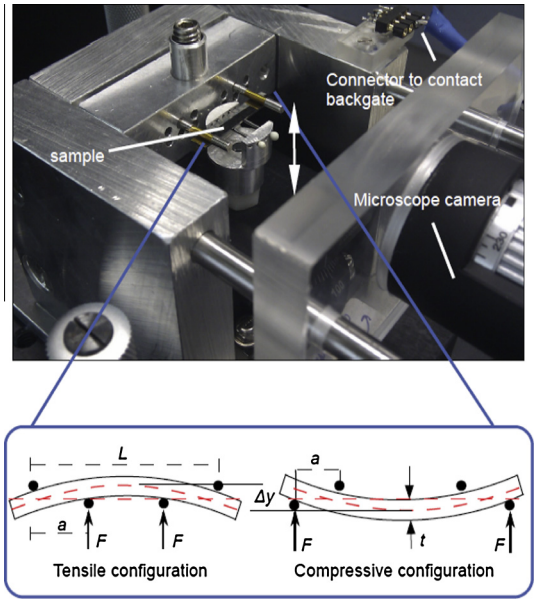

Fig. 4. View of the beam-bending experimental setup for tensile and compressive strain experiment.

the contact resistance R_c. Capacitance measurements $C(V)$ are performed to determine the C_{ox} value of the BOX.

The presence of the InAlAs barrier favors a confinement of the charge carrier in the active layer away of the BOX, with an expected reduction of the back-interface trap density and also a lesser impact of remote phonon scattering. This should allow a stronger mobility enhancement under strain and further downscaling of the InGaAs channel thickness at no performance loss. The distribution of the carrier density confined in the InGaAs layer separated from the Al_2O_3 BOX by the InAlAs barrier has been calculated using the 3D nano-device simulator Nextnano3 [11] (Fig. 5).

3. Results

The transfer characteristics of TLM structures with gate lengths L_G = 10–80 µm were recorded at V_{SD} = 50 mV and 1 V. The Ψ-MOSFETs investigated are based on the stack 25 nm $In_{0.53}Ga_{0.47}As$/0–10 nm InAlAs/35 nm Al_2O_3/Si with W electrodes. The channel is oriented along the [1 1 0] direction. The output characteristics for