



High voltage REBULF LDMOS with N^+ buried layer

Baoxing Duan^{a,*}, Yintang Yang^a, Bo Zhang^b

^a Key Laboratory of the Ministry of Education for Wide Band-Gap Semiconductor Materials and Devices, School of Microelectronics, Xidian University, No. 2 South TaiBai Road Xi'an, Shaanxi 710071, PR China

^b State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, No. 4 Section 2, North Jianshe Road, Chengdu, Sichuan 610054, PR China

ARTICLE INFO

Article history:

Received 7 May 2009

Received in revised form 4 February 2010

Accepted 8 March 2010

Available online 1 April 2010

The review of this paper was arranged by Prof. S. Cristoloveanu

Keywords:

LDMOS

REBULF

Buried layer

Breakdown voltage

ABSTRACT

A novel concept of REBULF (Reduced BULK Field) is proposed for the developing smart power integrated circuit with the thin epitaxy layer. The REBULF LDMOS structure is designed with N^+ buried layer embedded in the high-resistance substrate. The mechanism of breakdown of the new device is that the high electric field around the drain is reduced by N^+ buried layer, which causes the redistribution of the bulk electric field in the drift region of the REBULF LDMOS so that the substrate supports more biases. The critical condition of the REBULF technology is analyzed and validated by 2-D MEDICI simulation results, which is the product of the location of N^+ buried layer and substrate's doping is not more than $1 \times 10^{12} \text{ cm}^{-2}$. The breakdown voltage of REBULF LDMOS is increased by 75% in comparison to the conventional RESURF LDMOS from the simulation results. The experimental results show the high electric field around the drain is reduced as the depletion region spreads to N^+ buried layer. Although the leakage has increased a little, this increase is not enough to cause the avalanche breakdown.

Crown Copyright © 2010 Published by Elsevier Ltd. All rights reserved.

1. Introduction

In the LDMOS (Lateral Double-diffused MOSFET) device, the RESURF (ERduced SURface Field) technology had been presented for the power IC incorporating an n^- epitaxy layer on the silicon wafer to increase the breakdown voltage [1]. Several new structures had been developed on the basis of the RESURF technology [2–7]. In recent years, the power IC has emerged as an area for rapid growth in consumer and industrial applications. When the thin epitaxy layer is used, a self-isolating structure can be adopted in the power IC (PIC) to isolate low and high-side drivers, which is easy to be realized in semiconductor process [8]. A floating RESURF LDMOS structure has been proposed in Ref. [9] for the thin epitaxy technology. However, N^+ buried layer is embedded into P^+ substrate in this structure. The high breakdown voltage cannot be obtained due to the P^+ substrate. A new structure of the REBULF LDMOS had been designed with the high breakdown voltage for the power IC applications [10].

In this paper, a novel REBULF (Reduced BULK Field) LDMOSFET is designed with N^+ buried layer embedded in the high-resistance substrate for the development of smart power integrated circuit with the thin epitaxy layer. The breakdown voltage of this device is improved by reducing high electric field around the drain due to N^+ buried Layer which causes the redistribution of the bulk

electric field in the drift region. The results show using a 2-D device simulation MEDICI [11] the substrate supports more biases thanks to the effect of REBULF.

2. Device structure

Fig. 1 shows the schematic cross-section of the REBULF LDMOS with n^- -channel. A highly N^+ layer with n -type doping of which concentration is more than $1 \times 10^{17} \text{ cm}^{-3}$ is embedded in the high-resistance substrate, which dose not involved in the conventional structure. The potential of the N^+ layer is floated up when the depletion layer spreads into this region, thus the high electric field around the drain is reduced by the redistribution of the bulk electric field in the drift region, and the substrate supports more biases due to the parallel plane D_3 junction (shown in Fig. 1). The distance from the N^+ layer to the bottom of drift region is W which must be less than the thickness of depletion layer (W_p) in the substrate of the RESURF LDMOS. N_d , N_{p+} , N_{sub} are the concentration of the drift region, the channel and substrate, respectively, L_d is the length of the drift region, and T_s is the thickness of the drift region. The length of the source region and channel are $4 \mu\text{m}$ and $3 \mu\text{m}$ in the discussion of this paper.

3. Simulation results

Fig. 2 shows the simulated potential contours as the breakdown occur for the proposed REBULF LDMOS and optimal Buried layer

* Corresponding author at: 373# Key Laboratory of the Ministry of Education for Wide Band-Gap Semiconductor Materials and Devices, School of Microelectronics, Xidian University, Xi'an 710071, PR China. Tel.: +86 029 88204430.

E-mail address: bxduan@163.com (B. Duan).

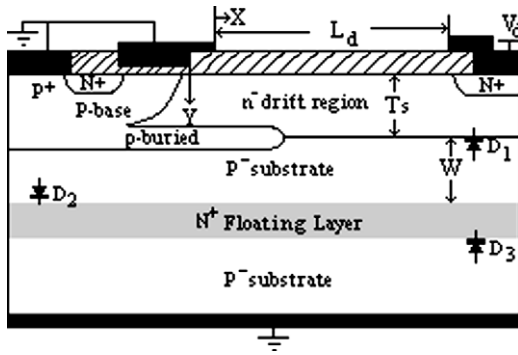


Fig. 1. Cross section of the REBULF LDMOS.

RESURF LDMOS structures with $2\ \mu\text{m}$ drift region. The drift region is doped according to the RESURF principle to achieve a maximum breakdown voltage. It is clear that the Buried layer RESURF LDMOS (shown in Fig. 2a) breaks down at the D_1 junction due to electric field crowding near the drain and breakdown voltage is limited to 331 V. However, in the REBULF LDMOS designed according to the REBULF effect (shown in Fig. 2b) a part of the potential contours are pulled out toward the source region due to the potential obtained by the N^+ floating layer. In this case the potential across the D_1 junction (shown in Fig. 1) has reduced significantly and the breakdown point of the REBULF LDMOS occurs under the source and D_1 junction simultaneously in the case of optimum, thus its breakdown voltage reaches 642 V.

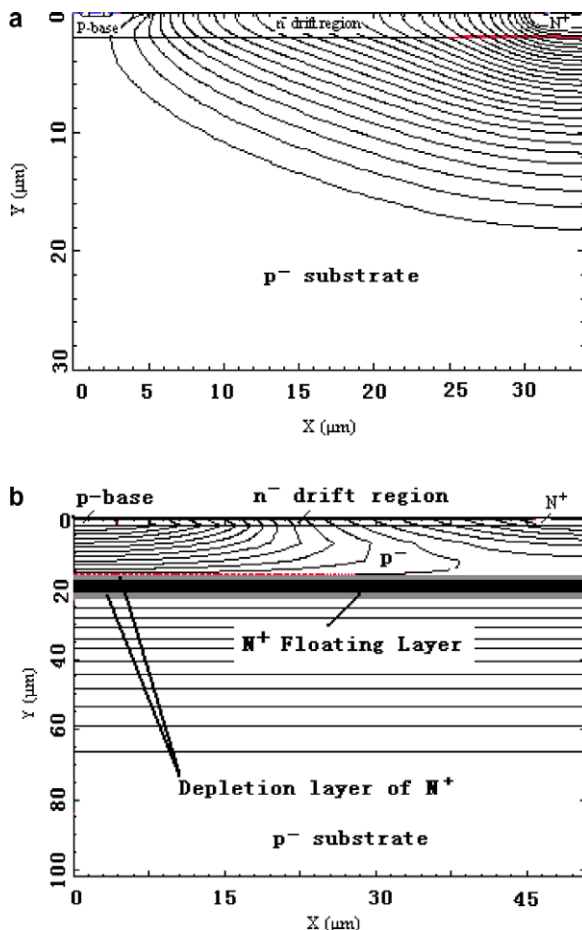


Fig. 2. Potential distribution of RESURF LDMOS (a) and REBULF LDMOS with the depletion layer of N^+ floating layer (b).

Fig. 3a shows the horizontal electric field distributions along the boundary of n^- drift region and p^- substrate. It is clear that a new electric field peak is brought in the RESURF LDMOS with p -type buried layer due to electric field modulation effect [2] by the p -type buried layer in comparison to the conventional LDMOS satisfied only single RESURF. This new field pulls down the height of electric field peak near the drain of the conventional LDMOS, which causes the breakdown voltage reaching 331 V for the RESURF LDMOS with p -type buried layer compared to 286 V in the conventional single RESURF LDMOS. It is apparent that this new field peak is developed in the REBULF LDMOS thanks to potential floating up by N^+ buried layer which increases the electric field around source by spreading the depletion layer into the source region, thus the electric field around drain does not reach the critical electric field when the voltage of the drain is 331 V which is the breakdown voltage of the Buried layer RESURF LDMOS. The breakdown voltage of REBULF LDMOS is improved to 642 V due to the REBULF effect.

The vertical electric field distributions around the drain were shown in Fig. 3b. Under the reverse bias condition, the electric field around the drain of the REBULF LDMOS is divided into two parts which were produced by D_1 and D_3 junctions. In this way, the maximal electric field around drain becomes lower than in the RESURF LDMOS. When the avalanche breakdown happened in the RESURF

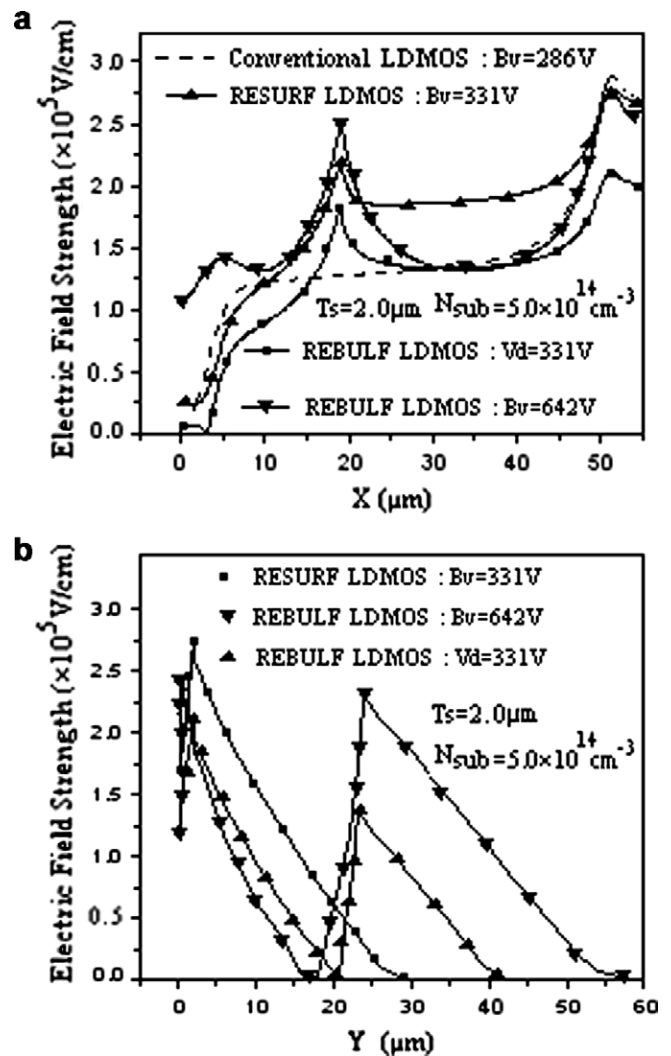


Fig. 3. Electric field distributions: (a) lateral electric field profiles along the boundary of n^- drift region and p^- substrate and (b) vertical electric field profiles around the drain.

Download English Version:

<https://daneshyari.com/en/article/747941>

Download Persian Version:

<https://daneshyari.com/article/747941>

[Daneshyari.com](https://daneshyari.com)