Solid-State Electronics 104 (2015) 61–69

Contents lists available at ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

Ultrafast lateral 600 V silicon SOI PiN diode with geometric traps for preventing waveform oscillation

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ARTICLE INFO

Article history:
Received 28 July 2014
Received in revised form 7 November 2014
Accepted 16 November 2014
Available online 9 December 2014

The review of this paper was arranged by Prof. S. Cristoloveanu

Keywords:
Diode
Waveform oscillation
Reverse recovery
Forward voltage drop
Geometric trap

ABSTRACT

An ultrafast lateral silicon PiN diode with geometric traps is proposed using a silicon-on-insulator (SOI) substrate with the traps. The proposed diode successfully suppresses waveform oscillation because the trapped hole suppresses electric field penetration and prevents the oscillation trigger known as "dynamic punch-through." Because of the short current path caused by the oscillation prevention, the reverse recovery speed was higher and the reverse recovery loss was strongly reduced. The proposed trap structure and design method would contribute to performance improvement of all power semiconductor devices including IGBTs and power MOSFETs.

1. Introduction

Efficiency improvement and the prevalence of power electronics apparatus are key factors for efficient energy usage in our more electric-oriented society [1,2]. For these key factors, fast switching, low forward voltage drop, and low cost are required for power semiconductor devices, because fast switching and low forward voltage drop increase the saved energy, while low cost reduces the system cost of power electronics.

To meet these demands, power semiconductor devices have made remarkable progress in recent decades and many technologies have been continuously studied to enable next-generation power electronics. These technologies are divided into three major areas: "more silicon (breakthrough in silicon power technology)," "beyond silicon (heterogeneous integration technology)," and "more than silicon (wide-bandgap power technology)".

Silicon devices are superior to wide-bandgap power devices in the aspect of low cost (mass production technology). On the other hand, it was believed that the physical properties of silicon make it difficult to make switching any faster. Therefore, many researchers have challenged the ultrafast reverse recovery and proposed a novel diode structure with a geometric trap concept in silicon power technology [3–13].

2. Potential and problems for faster reverse recovery

The reverse recovery speed and forward voltage drop are the main characteristics of diode performance. The forward voltage drop of the Si-PiN diode is determined by the sum of the built-in potential at the PN junction and the voltage drop in the N-layer. Similarly, the forward voltage drop of the SiC Schottky barrier diode (SBD) is determined by the sum of the Schottky barrier height at the metal–Si junction and the voltage drop in thin N-layer. The forward voltage drop of the Si-PiN diode is almost the same as that of the SiC-SBD. However, the reverse recovery speed of the Si-PiN diode is extremely slow because it takes a long time for the electric field to sweep the hole out of the N-layer.

Faster reverse recovery (faster switching) has a large impact not only on diodes but also on switching devices including IGBTs. This is because the reverse recovery current due to stored carrier of diode pass through switching device during turn-on and increase current peak of the switching device. So the turn-on loss of the switching device is strongly reduced with a fast reverse recovery diode (Fig. 1) [14,15].

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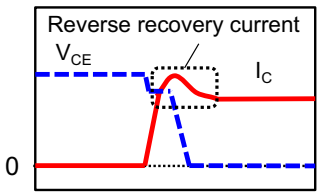
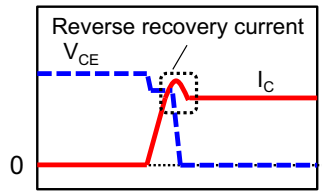
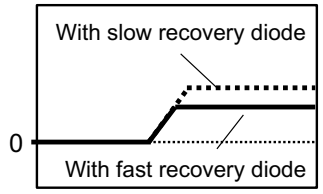
http://dx.doi.org/10.1016/j.sse.2014.11.011
0038-1101/



(a) Turn-on waveform of IGBT with slow recovery diode



(b) Turn-on waveform of IGBT with fast recovery diode



(c) Turn-on enery loss

Fig. 1. Image of reduced turn-on energy with fast recovery diode. (a) Turn-on waveform of IGBT with slow recovery diode. (b) Turn-on waveform of IGBT with fast recovery diode. (c) Turn-on energy loss.

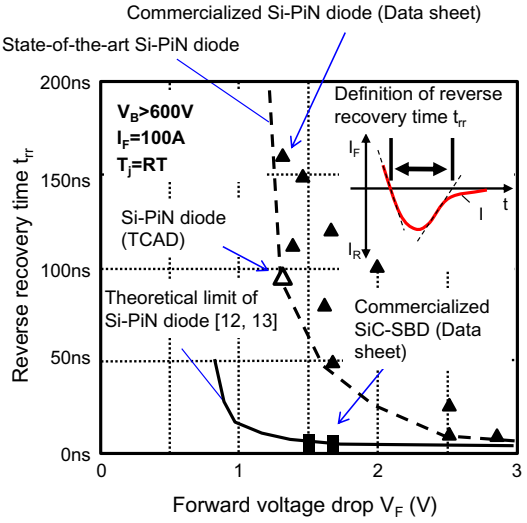


Fig. 2. Performance of state-of-the-art 600 V Si-PiN diode and benchmarks.

The authors calculated the reverse recovery speed by a bipolar device model and investigated the reverse recovery time of a state-of-the-art Si-PiN diode from a data sheet and TCAD simulation. The applied voltage is 300 V, current density is 250 A/cm^2, and stray inductance is 50 nH for TCAD simulation. It was found that there was a large potential for faster reverse recovery between the state-of-the-art commercialized diode and the theoretical limit (Fig. 2). The theoretical reverse recovery time limit is calculated with flat carrier distribution, so it is assumed that only drift current flows in the N-layer [16]. The potential reverse recovery speed was much higher than that of the state-of-the-art diode and was almost the same as the commercialized SiC-SBD [17]. Please note that the forward voltage drop (V_F) of electrode metal and bonding wires is not considered in this paper.

On the other hand, it was also revealed by the TCAD simulation that the fast reverse recovery of the Si-PiN diode having a thin N-layer induces a hard waveform oscillation during the reverse recovery time, as shown in Table 1. The waveform oscillation causes serious problems of conduction noise and emission noise. Because of the noises induced by the oscillation, the Si-PiN diode has not achieved ultrafast reverse recovery until now.

The phenomenon of oscillation trigger has been clarified in previous work [18–21]. When the carrier injection of the diode is stopped, the stored carrier is swept out from both sides of the thin N-layer (Fig. 3). At the same time, the high electric field penetrates from both sides and finally reaches the other high electric field. This phenomenon is the trigger for the waveform oscillation known as "dynamic punch-through." After the dynamic punch-through, the waveform is continuously oscillated by LC resonance with a stray inductance and a junction capacitance, because the hole as a resistance is completely swept out of the N-layer. Therefore, elimination of the dynamic punch-through is indispensable for the prevention of oscillation. The PiN diode having a thick N-layer is one of the typical methods to prevent the oscillation, because the hole remains throughout the reverse recovery and prevents the dynamic punch-through (Fig. 4). As a result, the waveform does not oscillate, although the reverse recovery speed becomes slower.

Previously proposed diodes for the oscillation suppression are roughly divided into two types; one type prompts reinjection of the carrier by the partial doping layer and the other prevents hard dynamic punch-through by an additional N layer in the N-layer [22–26]. However, these structures cannot achieve dramatic fast reverse recovery because the reinjection carrier or the additional N-layer slows reverse recovery.

3. Proposed ultrafast silicon PiN diode with geometric traps

This section describes the proposed diode structure and the fabrication process. The proposed diode shows the strong oscillation suppression effect with the unique mechanism. In addition, the authors propose a simplified design and arrangement method for the traps. Because of the oscillation suppression effect, the ultrafast reverse recovery was achieved as noted in Section 3.4.

3.1. Proposed diode structure and fabrication process

We propose a completely different diode, namely the lateral silicon-on-insulator (SOI) diode with geometric traps, as shown in Fig. 5. It has convexo–concave-shaped traps with Si and oxide on top of the buried oxide. The average thickness of the silicon and buried SiO_2 is 10 μm and 5 μm, respectively. The trap pitch and height are 5 μm and 0.5 μm, respectively.

The example of the fabrication process for convexo–concave-shaped traps had the following steps: local oxidation of Si (LOCOS) or oxidation after Si dry-etching, chemical mechanical polishing (CMP), and bonding. The fabrication process was similar to the conventional SOI structure. The fabrication process for the P emitter and anode electrode was adequately considered by a combination of boron diffusion and a deep reactive ion etching-like trench gate process. And about junction termination, dielectric separation