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Analysis of trap distribution in polysilicon channel transistors using the variable amplitude charge pumping method

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ABSTRACT

The trap distribution of a polysilicon (poly-Si) channel in a metal–oxide–semiconductor field effect transistor (MOSFET) was extracted successfully using a variable amplitude charge pumping method (VACP) and an energy band bending model. Compared to single crystal Si channels, the poly-Si channels exhibited a high density of bulk channel traps due to the presence of grain boundaries. The densities of the trap states existing in the poly-silicon channel with various grain sizes and channel thicknesses were extracted and compared. The grain size of poly-Si was found to have a stronger impact on the trap distribution than the channel thickness. After hot carrier stress, the trap density in the poly-silicon channel increases and the generated traps are located both at mid gap energy level and near the conduction band energy level.

1. Introduction

Through numerous studies, the drivability of devices with a polycrystalline silicon (poly-Si) channel has been improved considerably and poly-Si has been implemented successfully as a channel material in thin-film transistors (TFTs) of the active matrix in the flat panel displays industry [1,2]. Thus far, poly-Si is not attractive as a channel material in logic or memory applications because the grain boundaries in poly-Si inevitably lead to performance degradation and non-uniformity. On the other hand, the significant increase in the bit density in NAND flash memory has attracted increasing attention to the poly-Si channel. As the bit density increases, lateral device scaling in a conventional planar structure becomes increasingly difficult and new device structures, such as a vertical-stacked cell array including Pipe-shaped Bit-Cost Scalable (P-BiCS) [3,4], Vertical NAND (V-NAND) [5] and Terabit Cell Array Transistor (TCAT) [6,7], have been proposed. Because these 3-dimensional structures require poly-Si as a channel material, where the concentration of bulk traps inside the channel cannot be negligible, it is essential to evaluate the trap states in the grain boundaries precisely and improve the quality of the poly-Si channel by adopting the appropriate passivation techniques. To date, several extraction methods have been used to estimate the channel trap density [8], interface trap density [8,9], and grain boundary trap density [10,11] of poly-Si MOSFETs. The extraction techniques [8,9] were improved using more than one device characteristic (C–V and I–V). On the other hand, these models were not precise enough to determine the trap distribution because thermionic transport assumptions in channel carrier transport (I–V) between the source and drain junctions were used as the main input data [10,11] or boundary condition [8,9]. The charge pumping (CP) method [12–15] is used widely to determine the interface trap density in metal–oxide–semiconductor field effect transistors (MOSFETs) with a single crystal (SC) silicon channel because of its good detection limit and convenience [12]. It can also enable to estimate the trap generation induced by hot carriers with negligible detrapping [15]. However, few studies have used the charge pumping method to obtain the mean trap density within a channel of poly-Si MOSFETs [14,15]. The dependence of the trap density on the channel thickness could refer to an inaccurate evaluation of the quality of the channel material. In this study, the trap distributions in poly-Si MOSFETs with different thicknesses and grain sizes were obtained successfully using variable-amplitude charge-pumping

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(VACP) or amplitude-sweep charge-pumping (ACP) and an energy band bending model. The trap generation in the poly-Si channel under hot carrier stress (HCS) condition was also examined to confirm the validity of the extraction technique.

2. Experiment

Fig. 1 shows the top view and cross section view of the poly-Si TFT structure. Firstly, a 500 Å amorphous silicon (a-Si) layer was deposited on a 1000 Å SiO_2 layer by low pressure chemical vapor deposition (LPCVD) and patterned to reduce the contact resistance of the channel. Undoped amorphous-Si (a-Si) deposited by LPCVD was followed by solid phase crystallization (SPC). After using an active mask, 8 nm SiO_2 was deposited as a gate oxide. Another a-Si layer was deposited and patterned to be the gate. Phosphorous ions were implanted with the energy of 50 keV and dose of 10^{15} cm^{-2} to form source/drain contacts for MOSFET. The grain size was controlled by changing initial a-Si thickness (260 nm, 200 nm and 150 nm). Since the grains were formed by SPC, the grain sizes are proportional to the thicknesses of initial poly-Si films as reported [16]. The average grain sizes that were measured by electron backscattered diffraction (EBSD) are 550 nm (large grain), 470 nm (medium grain) and 400 nm (small grain), respectively. On the other hand, the channel thickness was controlled by etching so that the grain size was independent of the final poly-Si thickness [17]. In this study, we have used four types of poly-Si channel, large grain (23 nm and 18 nm in thickness), medium grain (18 nm in thickness) and small grain (9 nm in thickness,). Single crystalline (SC) silicon MOSFETs with the same dielectric were also prepared on a "silicon on insulator" ("SOI") wafer as the control sample.

Amplitude-sweep charge-pumping (ACP) [14] was carried out for both the poly-Si MOSFETs and SC silicon MOSFETs, W/L = 1 μm/1 μm. The charge pumping current from body contact was converted to the trap density per area (N_{CP}). The base voltage, V_{Base}, of the pulses applied to the gate was kept at −2 V. The N_{CP} values were obtained by varying the high voltage of the pulses, V_{High}. The pulses were applied on the gate with frequency f = 10 kHz, 1 μs in the rise time and fall time. This condition was selected to reduce the overestimation of charge pumping current, I_{CP} [17].

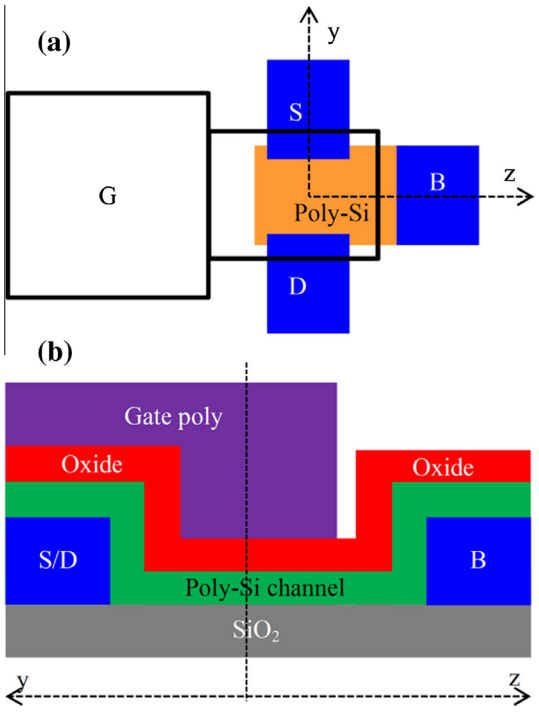

Fig. 1. Top view (a) and cross section view (b) of poly-Si TFT structure.

3. Theory

In the bulk MOSFETs, the bending of energy band is localized only near the oxide – channel interface. However, the energy band of ultra-thin channel must change during the gate voltage sweep due to the accumulation or fully depletion of carriers in the channel. Fig. 2a–c show the energy band structure of the poly-Si channel during the ACP measurements. At $V_{High} = V_{FB}$, which is the flat band voltage, Fermi level (E_F) lies on top of the intrinsic Fermi level (E_i) because the channel is non-intentionally-doped. When gate voltage (V_G) is smaller than V_{FB} at $V_G = V_{Base}$, the energy bands in poly-Si were bent upward (E_C, E_V and E_i) due to the hole accumulation, which means the E_i level is above E_F (see Fig. 2a). The trap states contributing to the charge pumping current are the states that are initially empty at $V_G = V_{Base}$ but filled at $V_G = V_{High}$. The shaded areas in Fig. 2a and b represent the energy states whose energy levels are higher than E_F at $V_G = V_{Base}$ but go down below E_F at $V_G = V_{High}$. When V_G increases from V_{Base} to V_{High} (in case of $V_{High} < V_{FB}$), the energy band in poly-Si moves downward but the E_i level is still above E_F (see Fig. 2b). In this case, N_{CP} comes from the trap states located in the region scanned by E_F that is indicated by the shaded area in Fig. 2b. If V_{High} becomes bigger than V_{FB}, N_{CP} includes not only the traps below E_i but also the traps above E_i (represented by the shaded area in Fig. 2c). These electron trap states, strongly affecting the n-type poly-Si MOSFETs performance, would be only filled when $V_G > V_{FB}$ – the trap energy states are below E_F. As a result, the density of the occupied electron traps above E_i and below E_F (N_{ET}) at $V_G = V_{High} > V_{FB}$ can be evaluated by $N_{ET} = N_{CP} - N_{CP}(FB)$, where $N_{CP}(FB)$ is the trap density extracted from the CP method when $V_{High} = V_{FB}$.

Fig. 2d illustrates the energy band structure in poly-Si MOSFET with dielectric and gate metal together when $V_G = V_{High} > V_{FB}$. ϕ_0 and ϕ_S are potential difference between E_F and E_i at the back interface and at the front interface, respectively. ϕ_S was calculated using quasi-static capacitance–voltage (QS-CV) measurements:

$$\phi_S = \int_{V_{FB}}^{V_G} \left(1 - \frac{C}{C_{ox}}\right) dV_G \tag{1}$$

where C, C_{ox}, and V_{High} (V_G) are the measured capacitance at $V_G = V_{High}$, the maximum capacitance, and gate voltage, respectively. QS-CV allows the response of trap states on a gate sweep, which is a good reference to monitor the effects of trapping in the poly-Si channel.

The electron trap distribution, D_{ET} (cm^{-3} eV^{-1}), in the poly-Si channel was introduced. This D_{ET} stands for the electron trap concentration at a particular energy region in the poly-Si channel. In the other words, D_{ET} is a function of the energy bending (ϕ) in the energy band structure and is assumed to be uniform along the poly-Si thickness. Since D_{ET} represents the value normalized by thickness, it can be an indication of channel quality. The electron traps located below the Fermi level are occupied and contribute to the total charge concentration, ρ, in the channel. The concentration of occupied electron traps above E_i at a certain point, x – distance to the back interface, in the channel, $N_e(x)$, was extracted using the following integration:

$$N_e(x) = \int_0^{\phi} D_{ET}(\phi) d\phi \tag{2}$$

The integration of $N_e(x)$ along the poly-Si thickness, N'_{ET}, presents the density of occupied electron trap states: