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Comparative study of electrical characteristics in (1 0 0) and (1 1 0) surface-oriented nMOSFETs with direct contact La-silicate/Si interface structure

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ABSTRACT

This study reports on the electrical characteristics of (1 1 0)-oriented nMOSFETs with a direct contact La-silicate/Si interface structure and the detailed comparison with (1 0 0)-oriented nMOSFETs. Precise control of oxygen partial pressure can provide the scaled EOT down to 0.73 nm on (1 1 0) orientation in common with (1 0 0) orientation. No frequency dispersion in C_{gc}–V characteristic for (1 1 0)-oriented nMOSFETs is successfully demonstrated at scaled EOT region, while higher amount of available bonds on (1 1 0) surface results in a larger interface state density, leading to the degradation of sub-threshold slope. High breakdown voltages of 2.85 V and 2.9 V for (1 0 0)- and (1 1 0)-oriented nMOSFETs are considered to be due to superior interfacial property. The electron mobility on (1 1 0) orientation is lower than that on (1 0 0) orientation because of the smaller energy split between fourfold valleys and twofold valleys as well as the larger density of states for lower-energy valleys in the (1 1 0) surface. Moreover, electron mobility is reduced with decreasing EOT in both (1 0 0)- and (1 1 0)-oriented nMOSFETs. It is found that threshold voltage instability by positive bias stress is mainly responsible for bulk trapping of electron even with a larger interface state density in (1 1 0) orientation and influence of surface orientation on threshold voltage instability is negligibly small.

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1. Introduction

Multi-gate structures combined with high-k/metal gate stacks has been implemented in CMOS technology, since continued scaling on conventional planar MOSFET has been becoming a significant challenge from a view point of tolerance to short channel effects [1]. In multi-gate structures, the short channel effect can be suppressed by decreasing the thickness of a body as the substitute for increasing channel doping, while severe degradation of mobility has been concurrently reported, resulting in degradation of performance [2]. Decreasing the body thickness is thought to be difficult with respect to shrinking the gate length and hence scaling in equivalent oxide thickness (EOT) should be continuously accomplished even in multi-gate devices for suppressing short channel effects. In this context, removal of SiO_2-interfacial layer (IL) in high-k/metal gate stacks is indispensable for reduction of the EOT because SiO_2-IL is typically formed to recover from the degradation of interfacial property or mobility [3,4]. A direct contact of high-k/Si interface structure is thus strongly required for multi-gate devices.

It has been reported that the direct contact of high-k/Si structure can be achieved with Hf-based oxides by sophisticated methods to scavenge SiO_x-based interfacial layer growth [4]. Moreover, an EOT of 0.62 nm accompanied by superior interfacial properties has been reported with a direct contact La-silicate/Si interface structure and an effective electron mobility of 155 $cm^2/V\,s$ has been demonstrated [5]. An advantage for La-silicate gate dielectrics is that the direct contact of high-k/Si structure can be easily achieved by simply depositing La_2O_3 on silicon (Si) substrate owing to the formation of La-silicate by the reaction between La_2O_3 and Si during annealing process [5].

Since (1 1 0) plane is usually utilized as the side-surface in FinFETs or tri-gate FETs coupled with (1 0 0) plane as top-surface [6], oxide/Si interface formed on (1 1 0) plane strongly contributes to the performance of multi-gate devices. As reactively-formed La-silicate dielectrics can easily provide the direct contact of high-k/Si interface, it is thus of great interest to investigate the electrical characteristics of MOSFETs fabricated on (1 1 0) orientation with direct contact of high-k/Si structure. In this paper, electrical characteristics for (1 1 0)-oriented nMOSFETs with direct contact of La-silicate gate dielectrics is studied through the comparison with

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(100)-oriented nMOSFETs to clarify the impact of surface orientation on nMOSFET characteristics. In order to distinguish the influence of surface orientation on device characteristics, planar MOSFET with (100) and (110) plane were prepared.

2. Device fabrication

La_2O_3 with 3 nm thickness was deposited on HF-last Si (100)- and (110)-oriented substrate by e-beam evaporation in an ultra-high vacuum chamber, followed by *in situ* W (tungsten) metal deposition by RF sputtering. The channel direction is parallel to ⟨110⟩. nMOSFETs were fabricated by gate last process using source and drain pre-formed p-Si substrates with a substrate doping concentration of 3×10^{16} cm^{-3}. TiN and Si were deposited on W metal by RF sputtering for scaled EOT [5]. The physical thickness of W, TiN and Si were 5 nm, 10 nm and 100 nm, respectively. Thermally-grown SiO_2 nMOSFETs was also fabricated with same substrate impurity concentration as references. The metal was patterned by reactive ion etching (RIE) with SF_6 chemistry to form gate electrodes. Post-metallization annealing were performed at 800 °C for 30 min in forming gas ambient (H_2:N_2 = 3%:97%) to form the La-silicate by the reaction with Si substrate [5]. Al was deposited on the source/drain region and back side of the substrate as a contact. Finally, recovery annealing was conducted at 420 °C for 30 min in forming gas ambient. Process flow and fabricated device structures are summarized in Fig. 1a and b.

3. Results and discussions

Fig. 2a and b compares the gate-to-channel capacitance (C_{gc}–V) between (100)- and (110)-oriented MOSFETs with deposited Si layers measured by split C–V method [7]. Almost same EOT of 0.75 nm and 0.73 nm can be obtained for (100)- and (110)-oriented MOSFET, respectively. Moreover, no frequency dispersion in C_{gc}–V characteristics are clearly observed in both (100)- and (110)-oriented MOSFET, indicating fairy nice interfacial properties. Fig. 3 shows the dependence of EOT on (100) and (110) orientation with various gate structures estimated from gate-to-channel capacitance. The oxygen partial pressure can be reduced by the deposited Si layer because the Si layer can prevent the diffusion of oxygen from atmosphere, enabling the scaled EOT [5]. As shown in Fig. 3, the EOT is decreased by lowering the oxygen partial pressure. It is found that the scaled EOT can be attained by controlling oxygen partial pressure regardless of Si substrate orientation. It has been reported that the oxidation rate of Si substrate is dependent on the surface orientation [8]. In the case of reactively-formed La-silicate gate dielectrics, no significant difference relating to the EOT between (100) and (110) orientation can be clearly confirmed as shown in Fig. 3. Formation rate of La-silicate is found to be almost identical irrespective of substrate orientation unlike with the oxidation of Si substrate. This result indicates that the conformal La-silicate layer might be realized. This same EOT of La-silicate gate dielectrics is likely caused by a radical-based interface reaction due to the catalytic effect of rare-earth oxides [9].

Next, the interface state density was evaluated by charge pumping method [10]. It is well known that the available bonds in (110) orientation are higher than that in (100) orientation, leading to larger interface state density [11]. Fig. 4a shows the

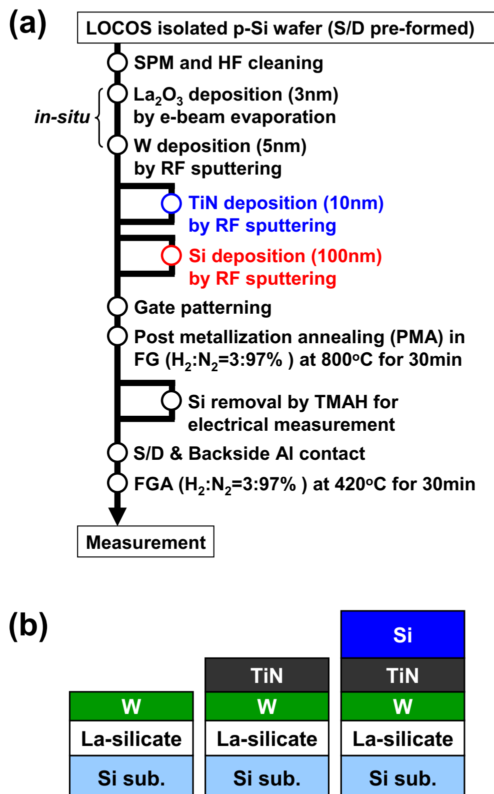

Fig. 1. (a) Process flow of nMOSFETs and (b) fabricated device structures, respectively.

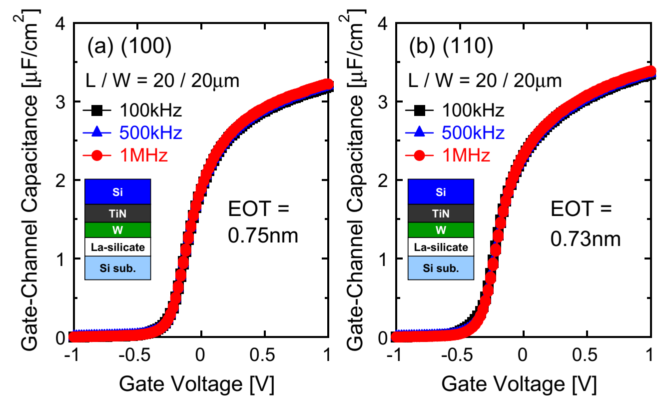

Fig. 2. Comparison of gate-channel capacitance for (a) (100)- and (b) (110)-oriented nMOSFETs with deposited Si layer, respectively.

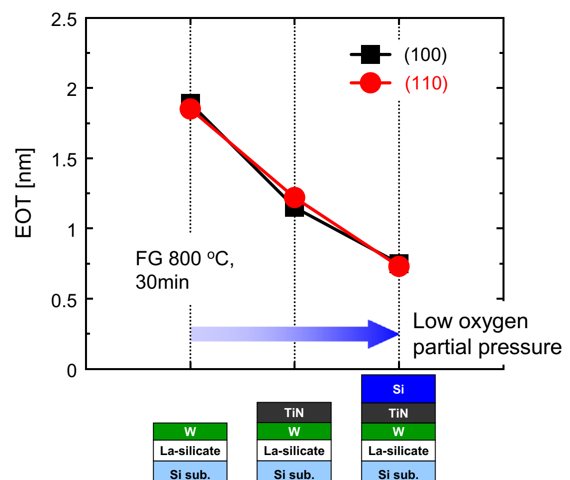

Fig. 3. Dependence of EOT on (100) and (110) orientation.

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