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$In_{0.53}Ga_{0.47}As$ FinFETs with self-aligned molybdenum contacts and HfO_2/Al_2O_3 gate dielectric

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ABSTRACT

InGaAs channel FinFETs with self-aligned molybdenum (Mo) contacts was demonstrated using a gate-last process. By realizing Mo contacts on *in situ* doped n^{++} InGaAs source and drain and self-aligned to channel, the FinFETs achieved series resistance of ~250 Ω μm, which is the lowest value reported-to-date for InGaAs non-planar n-MOSFETs. A FinFET with channel length of 500 nm and equivalent oxide thickness (EOT) of 3 nm has an on-state/off-state current ratio of $\sim 10^5$ and peak extrinsic transconductance of 255 μS/μm at drain voltage of 0.5 V. To further reduce EOT, atomic-layer-deposited HfO_2/Al_2O_3 high-*k* dielectric was integrated in InGaAs FinFETs. Good interface quality and small EOT of ~1 nm were achieved. Forming gas annealing (FGA) was used for drive current enhancement. A 300 °C 30 min FGA leads to ~48% increase in drive current as well as significant reduction of subthreshold swing, probably due to an improvement of the HfO_2/Al_2O_3/InGaAs interface quality.

1. Introduction

Indium Gallium Arsenide (InGaAs) has higher electron mobility than Silicon (Si) and is attractive as a channel material for n-channel metal-oxide-seminconductor field effect transistors (n-MOSFETs) [1–17]. InGaAs channel non-planar n-MOSFETs (FinFETs, Multiple-gate FETs, Tri-gate FETs, or Gate-all-around FETs) have improved control of short-channel effects (SCEs) than InGaAs planar n-MOSFETs and could be adopted as logic transistors in sub-10 nm technology nodes [18–24]. Several groups have demonstrated InGaAs channel non-planar n-MOSFETs in the past three years. However, there is still lack of research on source/drain (S/D) series resistance (R_{SD}) engineering for InGaAs non-planar transistors. R_{SD} comprises the parasitic source resistance (R_S) and drain resistance (R_D). By examining the state-of-the-art S/D contact technologies of InGaAs non-planar transistors (Table 1), it is noticed that a combination of *in situ* doped S/D and self-aligned contact could help to achieve significant reduction of R_{SD}.

A salicide-like CMOS-compatible self-aligned Ni–InGaAs metallization was recently developed for InGaAs FinFETs [23]. A R_{SD} of 364 Ω μm was reported, which is quite low compared to those of other InGaAs non-planar n-MOSFETs. This was primarily attributed to the low contact resistance (R_C) of Ni–InGaAs and self-alignment of Ni–InGaAs contacts to the gate stack. However, an analysis of the resistance components in Ref. [23] reveals that Ni–InGaAs has a R_C of 79 Ω μm. This means that $2R_C$ (which equals to 158 Ω μm) contributes a significant portion of ~43% to R_{SD} [23]. Therefore, reduced R_C between metal contact and n^{++} InGaAs is needed to further reduce R_{SD}. Another resistance component for the FinFET in Ref. [23] is the n^{++} InGaAs cap resistance ($2R_{cap}$ = 68 Ω μm). The n^{++} InGaAs cap is located between Ni–InGaAs contacts and InGaAs channel due to the gate-to-source/drain overlap. The n^{++} InGaAs cap resistance contributes ~19% to R_{SD} in Ref. [23]. Therefore, a FinFET structure with S/D metal contact self-aligned to the InGaAs channel is needed to reduce the resistance resulting from n^{++} InGaAs.

In the first part (Section 2) of this paper, non-alloyed molybdenum (Mo) is used as metal contacts for *in situ* doped n^{++} InGaAs S/D of InGaAs FinFETs. Mo contact gives very low R_C on n^{++} InGaAs [11,12]. A novel gate-last process was used to realize FinFETs with Mo contacts that are self-aligned to the InGaAs channel. Initial results were reported in Ref. [24], and a more detailed documentation of the work is provided here. R_{SD} as low as ~250 Ω μm was achieved and this is the lowest value reported-to-date for non-planar InGaAs channel n-MOSFETs.

Various high-*k* dielectrics have been investigated for InGaAs FinFETs to achieve good interfacial quality and small equivalent oxide thickness (EOT) [18–24] (Table 2). InGaAs FinFET with $TaSiO_x$ gate dielectric achieves a small subthreshold swing (*S*) of ~95 mV/decade and small EOT of 1.2 nm at a channel length (L_{CH}) of 60 nm [21]. Al_2O_3 also has good interface quality on InGaAs, but the

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Table 1
S/D contact technologies for InGaAs non-planar n-MOSFETs.

InGaAs non-planar devices	S/D doping method	Contact materials	Self-aligned contacts	R_{SD} (Ω µm)	Reference
FinFETs (Purdue, 2009)	Ion-implant	NiAuGe	No	1200	[18]
Multiple-gate (NUS, 2011)	Ion-implant	PdGe	No	~1000	[19]
Tri-gate (Intel, 2010 &2011)	*In situ* doped	Not-reported	No	Not-reported	[20,21]
Gate-all-around (Purdue, 2011)	Ion-implant	NiAuGe	No	1150	[22]
Multiple-gate (NUS, 2012)	***In situ* doped**	**Ni-InGaAs**	**Yes**	**364**	**[23]**
FinFETs (NUS, 2012)	***In situ* doped**	**Mo**	**Yes**	**250**	**This work**

Table 2
Gate stack technologies for InGaAs non-planar n-MOSFETs.

InGaAs non-planar devices	Deposition tool	High-*k* materials	EOT (nm)	*S* (mV/decade)	L_{CH} (nm)	Reference
FinFETs (Purdue, 2009)	ALD	Al_2O_3	2–3	200	100	[18]
Multiple-gate (NUS, 2011)	MOCVD	HfAlO	5~6	~230	~130	[19]
Tri-gate (Intel, 2010 &2011)	ALD	$TaSiO_x$	1.2	~95	~60	[20,21]
Gate-all-around (Purdue, 2011)	ALD	Al_2O_3	~4.5	150	50	[22]
Multiple-gate (NUS, 2012)	ALD	Al_2O_3	~3	169	50	[23]

dielectric constant of Al_2O_3 is only ~9 and is not high enough for aggressive EOT scaling. The smallest reported EOT for Al_2O_3 dielectric in InGaAs non-planar n-MOSFETs is still larger than 2 nm. To scale down EOT, a dual high-*k* HfO_2-on-Al_2O_3 stack (denoted as HfO_2/Al_2O_3) formed by atomic layer deposition (ALD) has been used in InGaAs planar n-MOSFETs. Good interface quality and small EOT can be achieved for HfO_2/Al_2O_3 due to the combined benefits of good interface quality of Al_2O_3 and high dielectric constant of HfO_2 [25–29]. Recent studies reveal that forming gas annealing (FGA) can further improve Al_2O_3 or HfO_2 dielectric quality by reducing the fixed oxide charge density (Q_f) as well as interface trap density (D_{it}) [30–33].

In the second part (Section 3) of this paper, the integration of HfO_2/Al_2O_3 in InGaAs FinFETs with small EOT of ~1 nm is reported. Forming gas annealing at 300 °C for 30 min was performed for the FinFETs to further improve the quality of HfO_2/Al_2O_3 dielectric. FGA leads to significant improvement of *S* and drive current.

2. InGaAs FinFETs with Mo contacts self-aligned to channel

2.1. Molybdenum contacts on n^{++} InGaAs

Transfer Length Method (TLM) test structures were fabricated for the extraction of Mo contact resistance R_C on n^{++} $In_{0.53}Ga_{0.47}As$. The starting substrate has a 100 nm thick n^{++} $In_{0.53}Ga_{0.47}As$ layer with doping concentration (N_D) of 5×10^{19} cm^{-3} formed on 300 nm thick undoped $In_{0.52}Al_{0.48}As$ layer grown on bulk InP. Fig. 1a shows the layout of a TLM structure. Contact spacing (*d*) varies from 5 to 200 µm. To fabricate TLM, the wafer was firstly dipped in hydrochloric acid (HCl:H_2O = 1:3) to remove native oxide on n^{++} InGaAs surface. After that, the sample was quickly loaded into a sputtering chamber for deposition of ~40 nm thick Mo. Ni pads with thickness of 300 nm were also deposited and patterned using a lift-off process, as shown in Fig. 1b. Next, Mo film was etched by Cl_2-based plasma using Ni as an etch mask (Fig. 1c). The final step for TLM fabrication is to form n^{++} InGaAs mesas by wet etch in a mixture of citric acid and hydrogen peroxide (H_2O_2) solution (Fig. 1c).

The fabricated TLM was electrically characterized. Fig. 2a plots total resistance (R_T) between two Mo contacts as a function of contact spacing *d*. The circles are experimental data and the solid curve is linear line fit. R_C extracted from the intercept (*d* = 0) is ~24 Ω µm, which is comparable to the value reported in Ref. [11]. Statistical plot in Fig. 2b compares the specific contact resistivity (ρ_C) of Mo and Ni–InGaAs on n^{++} InGaAs measured from a number of TLM structures. Mo contact shows ρ_C in the order of 1×10^{-7} Ω cm^2 and is about 10 times lower than that of Ni–InGaAs (1×10^{-6} Ω cm^2) [23].

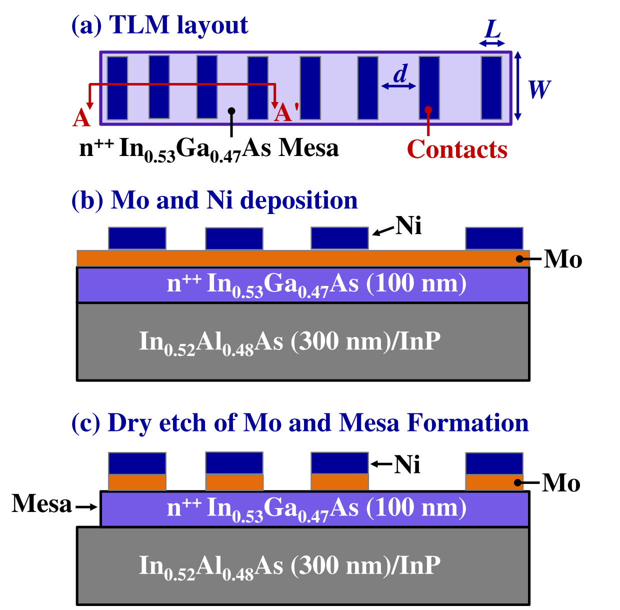

Fig. 1. (a) Layout of TLM test structure. *L*, *W*, *d* are contact length, width, and spacing, respectively. (b) Cross-section of the TLM structure along A–A′. Blanket Mo film was sputtered on the substrate, followed by deposition of Ni pads (300 nm) using a lift-off process. (c) Mo layer was etched in Cl_2-based plasma using Ni as an etch mask. Finally, n^{++} InGaAs mesa was formed by wet etch in citric acid based solution.

2.2. Integration of InGaAs FinFETs with Mo contacts self-aligned to channel

The process flow for the fabrication of InGaAs FinFETs with self-aligned Mo contacts is summarized in Fig. 3a. Bulk InP wafers served as the starting substrates. Sequential epitaxy of 300 nm of undoped $In_{0.52}Al_{0.48}As$, 50 nm of undoped $In_{0.53}Ga_{0.47}As$, 2 nm of undoped InP, and 30 nm of n^{++} $In_{0.53}Ga_{0.47}As$ ($N_D = 5 \times 10^{19}$ cm^{-3}) was performed. After native oxide removal in HCl solution, the