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Scaling of Trigate nanowire (NW) MOSFETs to sub-7 nm width: 300 K transition to Single Electron Transistor

V. Deshpande *, S. Barraud, X. Jehl, R. Wacquez, M. Vinet, R. Coquand, B. Roche, B. Voisin, F. Triozon, C. Vizioz, L. Tosti, B. Previtali, P. Perreau, T. Poiroux, M. Sanquer, O. Faynot

CEA-LETI, Minatec Campus and CEA-INAC, 17 rue des Martyrs, F-38054 Grenoble, France

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ABSTRACT

In this paper we show that on scaling nanowire width from 20 nm down to sub-7 nm regime, together with achieving excellent short channel effect control (DIBL = 12 mV/V for L_G = 20 nm), we hit a dramatic transition in transport mechanism from monotonously increasing I_D–V_G of a FET to oscillating I_D–V_G of a Single Electron Transistor. This transition in transport mechanism is brought about by process induced channel potential variability. It poses a challenge to further scaling of nanowire MOSFETs. However, we show that it provides an exciting opportunity to cointegrate Single Electron Transistors with high-k/metal gate operating at room temperature (at V_D = ±0.9 V) with the state-of-the-art nanowire MOSFETs enabling large scale manufacturing of *Beyond Moore* devices.

1. Introduction

Multigate FETs (MuGFETs) owing to their improved short channel effect (SCE) control are considered prime choice for next nodes [1,2]. Trigate NW-MOSFETs naturally form the successors to the current MuGFETs for extremely scaled gate lengths. Previous simulation works [3] have predicted a scaling law of $L_G \sim 3R$ (R – radius of NW) for reliable electrostatic integrity. So there is need for NW with channel diameter (or width for trigate), W = 3–5 nm at the end-of-roadmap. The main challenge for scaling nanowires to sub-10 nm channel dimensions was predicted to be threshold voltage (V_T) increase due to quantum confinement [3].

In this paper we first demonstrate performance of Trigate NW MOSFETs with width scaling down to 5 nm and then show, for the first time, that on scaling width from 20 nm to about 5 nm the transport properties can be completely modified: we evidence a transition from normal FET operation to SET operation at room temperature. In depth analysis with low temperature measurements is done to shed light on the physical phenomena at play. Besides this, it is also first time demonstration of cointegration of room temperature operating SET with NWMOSFET on state-of-the-art CMOS technology with high-k/metal gate.

2. Device fabrication

The full integration scheme developed by us for NWMOSFETs on SOI is shown in Fig. 1. Starting from a SOI substrate (T_{Si} = 12 - nm), NWs are patterned using 193 nm DUV lithography. We have two splits in NW width, W = 20 nm and W = 5–7 nm (based on CD measurements in SEM for various nanowires). Both of these width splits are achieved using resist trimming. This is the most important part of the integration scheme and details of this process will be described in the next paragraph. After the formation of active area (nanowires), high-k/metal gate stack comprising of 2.3 nm HfSiON, 5 nm ALD TiN and 50 nm poly Si is deposited. The pre-deposition cleaning is adapted to form an interfacial SiO_2 layer. Now gate down to 20 nm is patterned, again with DUV lithography followed by resist trimming and reactive ion etch (RIE). We use mesa isolation for the active areas, so the gate covers the nanowire on three sides making it 'trigate' geometry. After the gate is patterned, offset nitride spacers are formed. CD Spacer1 (shown in blue,[1] Fig. 1) = 25 nm for nanowires having width between 5 and 7 nm and CD Spacer1 = 10 nm for 20 nm wide NW. Silicon epitaxy is then performed on source/drain areas to obtain raised source/drain. LDD doping is performed thereafter. Now a second offset spacer (Spacer2) consisting of TEOS liner and nitride spacer is patterned. It is then followed by HDD doping to define source/drain and silicidation (with formation of NiPt silicide) for lower contact resistance. Tungsten contact and standard Cu back-end follows thereafter.

As mentioned before, most important part of the NWMOSFET integration is the active area patterning i.e. sub-10 nm width nanowire formation. We achieve this with 193 nm DUV lithography (DUV stepper tool) and resist trimming. The minimum pattern

* Corresponding author.
E-mail address: deshveeresh@gmail.com (V. Deshpande).

[1] For interpretation of color in Fig. 1, the reader is referred to the web version of this article.

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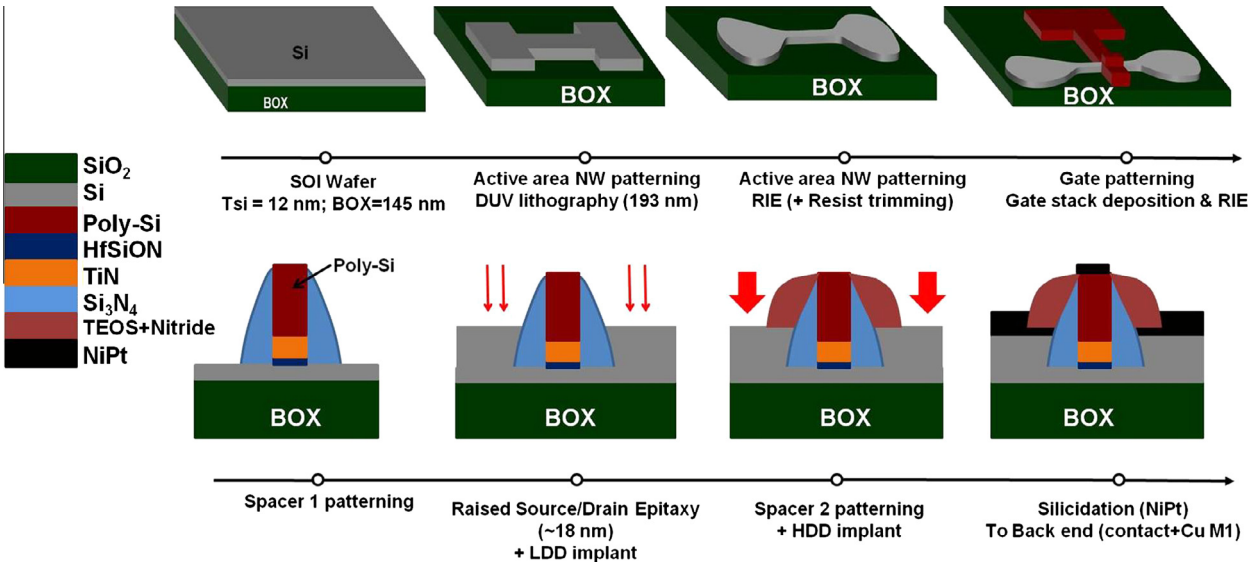

Fig. 1. Schematic of the NW-MOSFET integration scheme. Only the front-end process steps are shown. The back-end involves standard CMOS Cu back-end process.

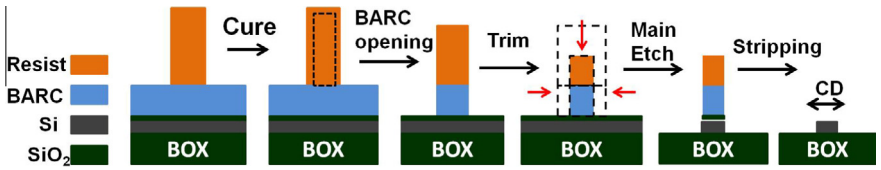

Fig. 2. The process sequence used for NW patterning through resist trimming.

width obtained after lithography is about 80 nm. The active stack used consists of undoped Si, SiO_2 dielectric layer, an organic bottom anti-reflective coating (BARC) layer and 193 nm ArF resist. The thickness of the photoresist is adapted to have proper aspect ratio at the end of trimming. The active zone (i.e. nanowire feature) etching is carried out using the trimmed resist/BARC as a mask. Obviously, the final line-width of nanowires is determined mainly by the amount of trimmed resist. Fig. 2 shows the process sequence used for NW patterning through resist trimming. First of all, HBr plasma curing process is performed in order to harden the 193 nm ArF resist for better etching resistance. Then, the BARC opening is done using CF_4 chemistry. This chemistry has been used in order to ensure vertical resist/BARC profile and correct line-width roughness. Moreover, as this sequence consumes a lot of photoresist, thickness of the BARC layer is well adapted to minimize the resist budget during the process. Then, the BARC/resist trimming process is performed just before the main etch to selectively pattern the silicon on the buried oxide. Trimming of the resist is performed to achieve nanowire structures down to nearly 5 nm in width using the HBr/O_2 plasma. Systematic width measurement for nanowires was carried out across full 300 mm wafer in a CD-SEM tool after active area etching step. Fig. 3a shows top view SEM image of NW for width split = 20 nm. For the other width split (5–7 nm), nanowires across wafer have width spread between 5 to 7 nm. Left part of Fig. 3b shows top view SEM image of 7 nm wide nanowire and the right part shows cross section TEM image (W = 7.6 nm). Observed width in TEM matches well and confirms CD-SEM top view measurements. As mentioned earlier, nanowires with even smaller width, down to about 5 nm have been measured. Fig. 3c shows top view SEM image of a nanowire with $W \sim 5$ nm (with relatively higher magnification). Fig. 3d shows SEM image of the gate after etching step.

3. Results and discussion

We will first discuss the electrostatic characteristics of the nanowire MOSFETs to establish their scaling behavior. Only those devices are considered in this section whose nanowire width has been measured systematically in CD-SEM after etching step. Hence the width values mentioned correspond to SEM measurements performed on them. Fig. 4a and b shows SCE control down to L_G = 20 nm for NMOS with nanowire width, W = 20 nm and W = 7 nm respectively. Nanowire width values mentioned here are the average of top view measurements performed with CD-SEM across a 300 mm wafer, after etching the nanowires (standard deviation of the width is about 1.5 nm). For gate length, L_G = 20 nm, drain induced barrier lowering (DIBL) and subthreshold swing (SS) are 30 mV/V and 72 mV/dec respectively for W = 20 nm. For the same L_G on reducing width to 7 nm, DIBL and SS are reduced to 12 mV/V and 62 mV/V respectively, showing excellent SCE control with width reduction. The I_D–V_G plots for L_G = 20 nm NMOSFETs with NW width = 20 nm and 7 nm are shown in Fig. 4c and d respectively. Though SCE control is already quite good for W = 20 nm nanowire, it is further improved on scaling width down to 7 nm. However, it can be seen that the ON state current of 7 nm nanowire is less as compared to 20 nm nanowire. This is due to larger CD of Spacer1 for 7 nm nanowires, which increases the access resistance. Thus we demonstrate Trigate NWMOSFETs with width of 7 nm that have excellent scalability and meet the requirements of end-of-roadmap node in terms of electrostatic control. Despite the excellent short channel effect control in NWs with W = 5-7 nm, we have observed a variability leading to peculiar characteristics in some devices. All the subsequent measurements are performed at 300 K (Figs. 5–8) unless specified. Fig. 5a shows the I_D–V_G characteristics of a NMOS with $W \sim 5$ nm (device A) with