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# Parameter set and data sampling strategy for accurate yet efficient statistical MOSFET compact model extraction

B. Bindu [a,*], B. Cheng [b], G. Roy [b], X. Wang [b], S. Roy [b], A. Asenov [b]

[a] Institute for Microelectronics, Technical University Vienna, Gusshausstrasse 27-29, A-1040 Vienna, Austria
[b] Device Modelling Group, Department of Electronics and Electrical Engineering, University of Glasgow, GlasgowG12 8LT, United Kingdom

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ABSTRACT

This paper presents an effective statistical compact modelling strategy that can precisely capture a statistical set of MOSFET characteristics into industrial strength statistical compact models. 3D simulation of large statistical sample of microscopically different devices is required for statistical compact model extraction when studying the impact of variability in next CMOS technology generations on circuit and system design. For a particular nominal device design the statistical 3D physical simulations needs two orders of magnitude more CPU time compared to conventional TCAD simulations. A data sampling strategy is presented to reduce the number of bias points in simulated device characteristics used as extraction targets for statistical compact model parameter extraction. We show that for a well balanced set of statistical compact model parameters carefully chosen small number of strategic bias points in the simulated *I–V* characteristics of each microscopically different transistor is sufficient to capture accurately the statistical device behaviour. The corresponding increase in the RMS error is below 1% compared to results from comprehensive bias point set. The impact of the slight reduction of the compact model accuracy on the accuracy of statistical circuit simulation has also been investigated.



## 1. Introduction

The purely statistical variability in the characteristics of MOSFETs, introduced by random discrete dopants (RDD) [1], line edge roughness (LER) [2], and poly gate granularity (PGG) [3] and other variability sources related to discreteness of charge and matter [4], is a major challenge for CMOS scaling and integration [5]. It is very important to be able to predict using comprehensive physical simulation the statistical variability in future technology generations and to accurately capture the results in statistical compact models since this is the only way to communicate this information to designers [6,7]. Previous research on statistical compact model identification was focused mainly on variability associated with traditional process variations resulting from poor control of critical dimensions, layer thicknesses and doping clearly related to specific compact model parameters [8,9]. Unfortunately, the current industrial strength compact models do not have natural parameters designed to incorporate naturally the truly statistical variability associated with RDD, LER, PGG and other relevant variability sources. Despite some attempts to identify and extract statistical compact model parameters suitable for capturing statistical variability introduced by discreteness of charge and matter, this remains an area of active research [10,11]. The problem is exacerbated by the complexity and the computational intensity of the statistical 3D physical simulation needed to provide the target characteristics for the statistical compact model extraction when studying future technology generations [12]. Many CPU hours are needed to generate the target *I–V* curves for an individual transistor from a statistical sample and the sample size ranges from hundred to thousand microscopically different transistors. In such circumstances the optimum selection bias point condition in the target *I–V* characteristics, which will give an acceptable compromise between computing time and compact model accuracy is very important.

In this paper, we investigate the optimal statistical parameter identification and data selection strategy in the statistical compact model extraction, quantifying the trade-off between the accuracy and computational burden. The paper is arranged as follows: Section 2 briefly describes the statistical physical device simulation used to generate the target *I–V* characteristics. Section 3 describes our generic statistical compact model parameter identification and extraction strategy. Section 4 describes the impact of different bias point selection strategies on the statistical compact model accuracy and the impact of data sampling strategy on

* Corresponding author. Tel.: +43 1 58801 36049; fax: +43 1 58801 36099.
*E-mail addresses:* binduboby@gmail.com (B. Bindu), b.cheng@elec.gla.ac.uk (B. Cheng), s.roy@elec.gla.ac.uk (S. Roy), a.asenov@elec.gla.ac.uk (A. Asenov).

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the circuit simulation accuracy. The conclusions are drawn in Section 5.

## 2. 3D statistical variability simulations

The simulations are carried out using the Glasgow 'atomistic' device simulator described elsewhere [13]. Special attention is paid to the accurate resolution of individual discrete dopants through simultaneous density gradient quantum corrections for electrons and holes [1]. The simulator supports automatic generation of single and combined variability sources [14]. It also automatically farms the simulations of the statistical sample in cluster or Grid™ computing environment and harvests the statistical results in databases allowing flexible statistical analysis [15].

The tested device in this study is a 35 nm physical gate length n-channel MOSFET with the performance match recently published state of the art 45 nm technology generation device results [16,17]. The TCAD [18] doping profile, generated by Sentaurus process simulation, which includes halo implants (inset in Fig. 1), and stress enhanced mobility values are fed into our in-house drift-diffusion (DD) 'atomistic' device simulator, which features density gradient (DG) quantum corrections, to produce device characteristics for compact model parameter extraction. The in-house simulator accurately captures device electrostatics and thus variability effects in the sub-threshold regime. It should be recognised that DD simulations can underestimate on-current variations. RDD, LER, and PGG which are the dominant sources of statistical variability in n-channel MOSFET, are included simultaneously in the simulation of a square 35 nm × 35 nm transistor. RDD is generated from the continuous doping profile obtained from TCAD simulation by placing dopant atoms on silicon lattice sites, with the probability determined by the local ratio between the dopant and the silicon atom concentration [1]. The parameters used to introduce LER in the simulations are correlation length $\Lambda$ = 30 nm and RMS amplitude $\Delta$ = 1.3 nm [2]. An average poly-silicon grain diameter of 65 nm, and the Fermi level pinning 0.35 eV below the conduction band are used to introduce the PGG [19]. Fig. 1 shows the spread in $I_D$–$V_G$ characteristics obtained from 'atomistic' simulator due to the combined effect of RDD, LER and PGG at high (1.0 V) drain bias condition. The threshold voltage standard deviation is $\sigma V_T = 56.3$ mV and the standard deviation of $I_{on}$ is 8.4% of its mean, where $I_{on}$ is defined as the drain current at $V_G = V_D = V_{DD} = 1.0$ V, $V_{DD}$ being the supply voltage. Fig. 2 shows a typical potential profile introduced by combined RDD, LER, and PGG variability sources where surface potential fluctuation can be clearly identified.

## 3. Compact model strategy

Predictive physical simulation of statistical variability and its capturing in accurate statistical compact modelling (SCM), is critical for design. Today designers need to know accurately the statistical variability far ahead of the introduction of particular technology generation, then only the statistical device variability can be reliably measured. Also commonly used SCM approaches usually assume simple normal distributions for the statistical compact model parameters and neglect their correlation [20]. This can result in compact model sets producing physically incorrect device characteristics, which can skew the statistical circuit analysis. Such approach also does not allow a critical backward analysis that can trace particular circuit behaviour to a particular 'anomalous' device characteristic and its physical origin. The presented here SCM extraction and utilisation strategy addresses the above deficiencies and is designed to be used as a 'gold standard' for benchmarking of other SCM strategies. The industry standard BSIM4 compact model [21] is employed in this study and the statistical extraction of compact model parameters is done in two stages [11]. In the first stage, one complete set of BSIM4 parameters is extracted from the *I–V* characteristics of 'uniform' (continuously doped, no RDD, LER and PGG) set of devices with different channel lengths and widths and process flow identical to the one of the 35 nm tested transistor. Target current voltage characteristics are simulated over the complete device operating range and parameter extraction strategy combining group extraction and local optimization is employed. Fig. 3 compares the corresponding BSIM4 generated *I–V* characteristics of the 35 nm MOSFET with the original device characteristics

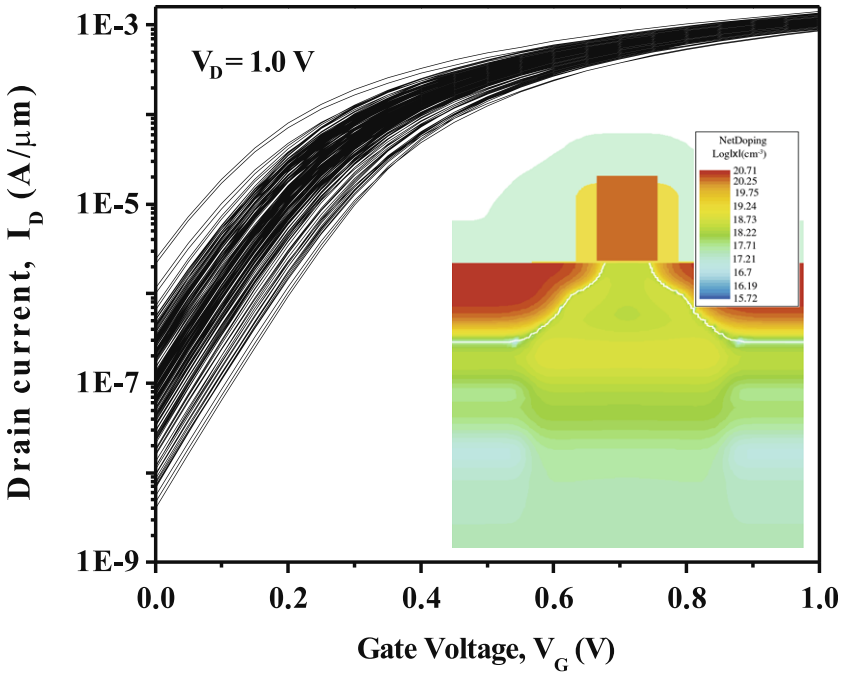


**Fig. 1.** Gate characteristics of 200 macroscopically identical 35 nm MOSFETs obtained from 'atomistic' device simulator. Inset: device structure of 35 nm physical gate length n-channel MOSFET.