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Reconfigurable nanowire electronics – A review ☆

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ABSTRACT

Reconfigurable nanowire transistors merge the electrical properties of unipolar n- and p-type FETs into a single type of device with identic technology, geometry and composition. These four-terminal nanowire transistors employ an electric signal to dynamically program unipolar n- or p-type behavior. More than reducing the technological complexity, they open up the possibility of dynamically programming the functions of circuits at the device level, i.e. enabling a fine-grain reconfiguration of complex functions. We will review different reconfigurable concepts, analyze the transport properties and finally assess their maturity for building circuits.

1. Introduction

The functional extension of switching elements is an alternative approach to classical scaling towards conceiving circuits and systems with added computational value. Skillfully implemented multifunctional devices that bear highly adaptable logic and computational blocks hold the promise of further advancing electronics and Moore's Law [1] even beyond the end of classical scaling [2–4]. Reconfigurable field effect transistors (RFETs) are such novel multifunctional or functionality enhanced devices that provide both, n- and p-FET characteristics as selected simply by an electric signal. These four-terminal nanowire devices rely on the unique properties of nano-scale Schottky junctions in nanowires to adjust the charge carrier polarity and concentration. In contrast to classical MOSFETs, RFETs do not require doping. In this manuscript we will review the progress and current status of reconfigurable nanoelectronics and will summarize the current challenges and opportunities that arise with this new paradigm. At first we will elucidate the electric characteristics and working principle of the RFET. We will further compare this device with alternative reconfigurable nano-devices. The physical working mechanism will be described in detail, through device simulations and nanoscopic transport experiments. We will finally proceed to discuss the potential of RFETs in building energy efficient circuits and systems.

The paper is organized as follows. Section 2 will motivate the need and list important requirements for reconfigurable transistors. Section 3 will elucidate the working principle and illustrate the electric characteristics of a specific type of reconfigurable transistor, the RFET with selective charge carrier injection. Section 4 will deal with different strategies for the adjustment of RFETs with the aim of obtaining symmetric *I–V* characteristics as required for complementary operations. Section 5 will show further realizations of re-configurability in 1-D transistors. The electronic transport properties will be analyzed by measurements and simulations in Section 6. Complementary circuits built from RFETs will be shown in Section 7. The capability of adapting the function of logic gates by a fine-grain configuration of the RFETs built within is described in Section 8. A performance and power indicator assessment will finally be given in Section 9. Opportunities and major challenges will be summarized in the conclusions.

2. In search of the universal CMOS switch

Energy efficient complementary metal oxide semiconductor (CMOS) circuits as studied and implemented over the last five decades have relied on integrated electron (n-type) and hole (p-type)

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conducting FETs with static switching functions [5]. The transistor pairs are able to connect and separate the potential of the logic node with a respective *pull-up* network to the supply voltage, V_{dd}, and with a *pull-down* network to the ground level, GND. The different polarity of the charge carriers in the complementary FETs is decisive to alternate switching of p- and n-type FETs during a single gate-voltage swing. Thereby the major power consumption occurs at the switching event. In comparison the static power consumption is small. The recent advances in nanometer scale electronics have enabled the conception of novel FETs that exhibit n- and p-type programmable functions from the same device. This lifts the necessity of having circuit building blocks with a predefined polarity at a specific location in electronic systems. Accordingly, novel and disruptive circuit schemes are necessary to benefit from the higher functionality and to tackle the inherent overhead of control signals present, compared to conventional CMOS.

An electronic switch that *universally* delivers n- and p-type operation upon demand has to fulfill a series of requirements to be applicable to build circuits and systems. These will be addressed in this paper and can be summarized as follows:

(A) Reversible configurability as p/n-type FET.
(B) Symmetric *I-V* characteristics of p/n-type FET.
(C) Sufficient drivability strength for neighboring FETs.
(D) Single supply voltage.
(E) Scalability.

In general, the charge carrier type that flows through conventional FETs is selected by the doping profiles, e.g. *n–p–n/n–i–n* for n-channel and *p–n–p/p–i–p* for p-channel. As device dimensions are continued to be reduced and 3-D channel structures are implemented, an accurate and reproducible control of the doping distribution [6] and doping efficiency [7,8] is of increasing difficulty. In contrast to doping, the first requirement listed above (A) *Reversible configurability as p/n-type FET*, involves that electrons and holes are to be injected into the intrinsic or lowly doped channel from the source and drain electrodes. Therefore, it becomes mandatory to replace the highly doped source and drain (S/D) regions of conventional FETs with metallic contacts that ideally align their work function near the mid-energy of the channel's band gap. Moreover, the first requirement calls for a mechanism for selective filtering or preferential injection of charge carriers depending on the desired polarity. Different realization procedures have been presented recently and are summarized and compared in the next section. At the course of this paper it will become clear that the nanowire RFET concept with individual source/drain gating does fulfill all requirements listed above.

3. The reconfigurable nanowire FET

Recently, several reconfigurable transistor concepts have been reported. These have employed different nano-scaled and low-dimensional channel materials such as intrinsic or lowly doped silicon [9,12,13,16,17], carbon nanotubes (CNT) [14] and graphene [15]. In all cases Schottky junctions were provided at S/D and a gate potential was used to directly induce band bending at the Schottky interface providing predominant charge carrier injection into the valence or conduction bands. In contrast to the case of bulk materials, the low-dimensional geometry of the semiconductors employed promotes efficient electrostatic control of the active region. In the case of silicon nanowires the formation of sharp metal/semiconductor interfaces is enabled. Three different types of reconfigurable device concepts exist, depending on the control of charge carrier selection and concentration:

(A) Selective charge carrier injection and concentration control at contacts.
(B) Polarity selection at contacts and control of charge concentration in channel.
(C) Ambipolar operation with charge carrier filtering in the channel.

Fig. 1 depicts a schematic and scanning electron micrograph of the concept (A). An overview of the three different concepts is given in Fig. 2. In the concept (A), *Selective charge carrier injection and concentration control at contacts*, selective carrier injection and control of charge carrier concentration take place directly at the source and drain contacts. To this end, the Schottky source and drain junctions are gated independently from each other and no gating in the middle of the channel is needed. One gate can block the undesired charge carriers prior to their entrance to the channel, thus programming the device polarity. The other gate is used to tune conductance of the other charge carrier kind. This device was first introduced and proven by the authors as a concept in 2008 [9] employing nominally intrinsic silicon nanowires grown by the vapor liquid solid (VLS) growth mechanism [10,11]. There Ta_2O_5 and Al_2O_3 high-k dielectrics were employed. These devices exhibited at that development stage a high interface state density at the Si/oxide interface and high charge trapping density, limiting efficient gating and introducing hysteresis in the IV characteristics. Significantly improved electrical characteristics, e.g. drive currents, were shown in [12] by incorporating a thermally grown SiO_2 layer. Recently, a breakthrough was reached by the same group later on [13], by showing fully symmetric electrical characteristics of RFETs and complementary circuits built out of these.

In the second approach, (B) *Polarity selection at contacts and control of charge concentration in channel* [14–17] both Schottky junctions are steered simultaneously accumulating either holes ($V_g < 0$) or electrons ($V_g > 0$) in the channel and thus programming the

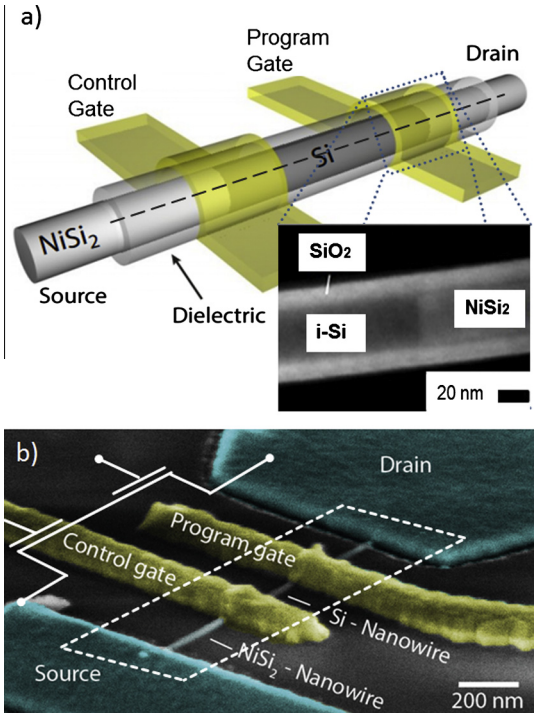

Fig. 1. The reconfigurable silicon nanowire FET with independent junction gating. (a) Schematic of the device. Two independent gates are positioned on top of the source and drain junctions. Inset shows SEM of typical cross-section at the Schottky contacts, exhibiting abrupt junction with well defined area. (b) SEM image of device after top gate deposition. Inset depicts device symbol.