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# Performance evaluation of parallel electric field tunnel field-effect transistor by a distributed-element circuit model

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ABSTRACT

The performance of parallel electric field tunnel field-effect transistors (TFETs), in which band-to-band tunneling (BTBT) was initiated in-line to the gate electric field was evaluated. The TFET was fabricated by inserting an epitaxially-grown parallel-plate tunnel capacitor between heavily doped source wells and gate insulators. Analysis using a distributed-element circuit model indicated there should be a limit of the drain current caused by the self-voltage-drop effect in the ultrathin channel layer.

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## 1. Introduction

Recently, there is a social need to reduce the power consumption of the electronic devices. Reducing the operation voltage of microchips to reduce their power consumption is an effective way [1]. However, the reduction in operation voltage of the conventional metal oxide semiconductor field-effect transistors (MOSFETs) used in today's electronic circuit is reaching the fundamental limit. The subthreshold swing (SS) of the MOSFET is limited to 60 mV/decade, which is governed by the operation mechanism of the MOSFET [2]. This makes it difficult to substantially reduce MOSFET operation voltage. To break through the limit, the tunnel FET is attracting attention as a novel low power-consumption devices.

Because the TFET utilizes band-to-band tunneling (BTBT) of semiconductors as an operation principle, it has a steeper SS than conventional MOSFETs [3–11]. However, the drain current of a TFET is several orders smaller than that of a MOSFET, which is a serious drawback in application to the circuit. Several techniques have been adopted to increase the drain current. The tunnel probability can be enhanced effectively with an abrupt source/channel dopant profile or by using direct-transition semiconductors. In addition, there are techniques to improve electrostatic controllability of the gate by modifying the TFET architecture. A TFET with tunneling parallel to the gate electric field is one such approach, which initiates BTBT in-line to the gate electric field [10,12–14]. The tunnel area can be increased by using such architecture. We have already reported enhancement of the drain current in parallel electric field TFETs [14,15]. In the present study, the effectiveness of the performance improvement of a parallel electric field TFET was experimentally evaluated, and analyzed using a distributed-element circuit model.

## 2. Experimental procedure

Fig. 1(a) and (b) shows respective schematic models for conventional (lateral) and parallel electric field (PE-) TFETs fabricated on silicon-on-insulator (SOI) wafers. The PE-TFET features an ultrathin parallel-plate (PP) tunnel capacitor inserted between the source well and gate insulator layer. Parallel BTBT transport is initiated in the TFET to the gate electric field. The PP capacitor overlaps with the source and gate regions, in which the overlap length is indicated by $L_{OV}$. Fig. 1(c) shows a simulation of the energy band diagram across the PP capacitor, calculated using the SILVACO-ATLAS TCAD simulator [16]. The potential modulation by the gate electric field initiates energy band modulation.

Fig. 2 shows a schematic process flow for fabrication of the TFET. SOI wafers with 75 nm thick SOI and 145 nm thick buried oxide (BOX) layers were used. The source and drain regions are

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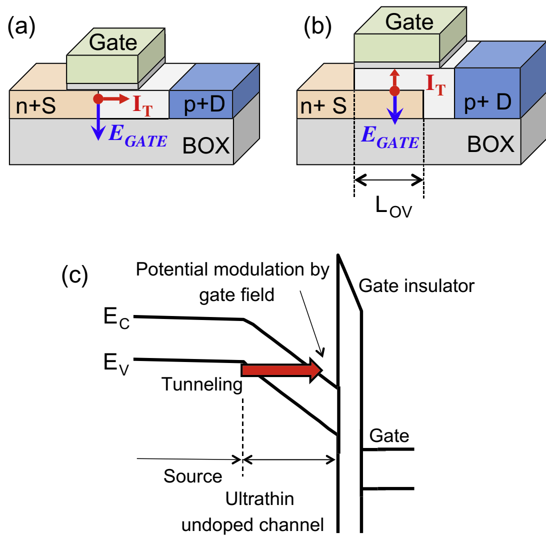


**Fig. 1.** Schematic models for (a) conventional and (b) parallel electric field TFETs. In (b), the tunneling direction ($I_T$) is in-line to the gate electric field ($E_{GATE}$). The overlap length ($L_{OV}$) is shown. (c) TCAD simulation of energy band diagram for parallel electric field TFET. $E_C$ and $E_V$ indicate the conduction and valence bands, respectively.

preferentially created by P or $BF_2$ implantation with a $2 \times 10^{15}$ $cm^{-2}$ dose at 6 keV, followed by activation annealing at 1000 °C. The epitaxial growth technique was used to fabricate the ultrathin PP capacitor. Epitaxial growth was performed in an ultrahigh-vacuum-based chemical vapor deposition chamber using $Si_2H_6$ and $H_2$ at 500 °C. After the epitaxial growth of undoped Si layer, $HfO_2/Al_2O_3$ layers were deposited by atomic layer deposition with no interfacial $SiO_2$ layer. A 40 nm thick TiN gate electrode was deposited by sputtering. After gate patterning, contact formation, and $H_2$ sintering, the electrical properties were measured.

Front-side secondary ion mass spectroscopy analysis showed an extremely steep (ca. 1.5 nm/decade) doping gradient between the highly doped source and undoped epitaxial channel [14,15]. Fig. 3(a) shows a typical cross-sectional transmission electron microscopy (X-TEM) image of the TFET equipped with the PP tunnel capacitor, in which the source and drain wells are highlighted by dashed areas. The physical gate length ($L_G$) and source overlap length ($L_{OV}$) are 120 and 50 nm, respectively. Between the source area and the high-k gate insulator, an ultrathin (2 nm thick) Si channel is inserted as the PP capacitor. Fig. 3(b) shows a magnified image of the TiN/high-k/epitaxial channel/SOI stack structure. The image of the SOI lattice shows a continuous connection to that of the thin Si channel, which indicates that the Si channel is epitaxially grown on the source Si surface.

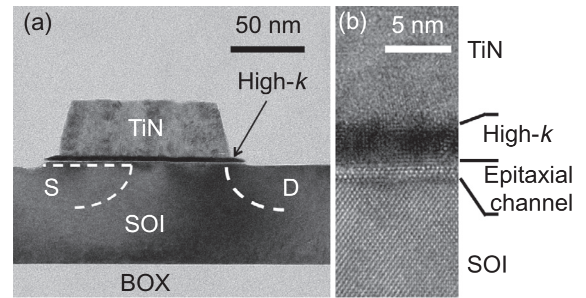


**Fig. 3.** Typical X-TEM images of (a) epitaxial channel TFET and (b) magnified TiN/high-k/epitaxial channel/SOI stack. Dashed lines indicate the preferentially implanted source and drain regions.

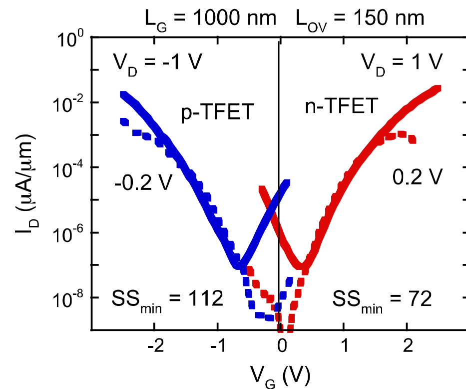


**Fig. 4.** Typical $I_D$–$V_G$ characteristics of p- and n-TFETs with PP tunnel capacitor for $V_D$ = |0.2| (dashed curves) and |1.0| V (solid curves), respectively. The EOT of the high-k gate insulator is 1.3 nm.

## 3. Results

Fig. 4 shows the $I_D$–$V_G$ characteristics for the p- and n-types PE-TFETs in the present study. The TFETs exhibited a symmetric on/off operation. The CMOS TFETs also exhibited inverter operation [14]. Fig. 5 shows the $I_D$ values for p-TFETs with different (0 and 40 nm) $L_{OV}$ lengths. The TFET with longer $L_{OV}$ have a larger drain

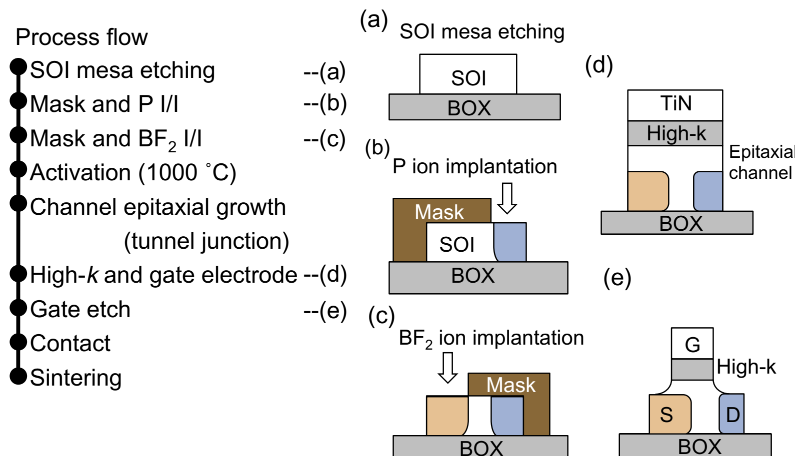


**Fig. 2.** Schematic process flow for the fabrication of a TFET with a PP tunnel capacitor. The epitaxial growth technique was used to fabricate ultrathin PP capacitor.

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