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Integration techniques of pHEMTs and planar Gunn diodes on GaAs substrates

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ABSTRACT

This work presents two different approaches for the implementation of pseudomorphic high electron mobility transistors (pHEMTs) and planar Gunn diodes on the same gallium arsenide substrate. In the first approach, a combined wafer is used where a buffer layer separates the active layers of the two devices. A second approach was also examined using a single wafer where the AlGaAs/InGaAs/GaAs heterostructures were designed for the realisation of pHEMTs. The comparison between the two techniques showed that the devices fabricated on the single pHEMT wafer presented superior performance over the combined wafer technique. The DC and small-signal characteristics of the pHEMTs on the single wafer were enhanced after the use of T-gates with 70 nm length. The maximum transconductance of the transistors was equal to 780 mS/mm with 200 GHz maximum frequency of oscillation (f_{max}). Planar Gunn diodes fabricated in the pHEMT wafer, with 1.3 μm anode-to-cathode separation (L_{AC}) presented oscillations at 87.6 GHz with maximum power of oscillation equal to −40 dBm.

1. Introduction

The first planar Gunn diodes presenting oscillations above 100 GHz [1] demonstrated the capability of integrating millimeter-wave sources with monolithic microwave integrated circuits (MMICs). The development of the device in subsequent years was focused on the modification of the layer structure for the reinforcement of the power performance since the initial diodes presented relatively low generated power equal to −43 dBm. The generated power was doubled and the phase noise significantly decreased after the introduction of extra delta-doping layers [2]. The introduction of $In_{0.23}Ga_{0.77}As$ channel layers led to an increase of the maximum oscillation frequency to 116 GHz [3]. Lately, planar Gunn diodes based on an $In_{0.53}Ga_{0.47}As$ channel layer presented significantly improved performance where the maximum frequency of oscillation was equal to 164 GHz with −10 dBm maximum power generated [4].

Alternatively, enhancement of the oscillator performance can be achieved by the monolithic implementation of the planar Gunn diode with transistor-based MMICs. Transmitters and receivers operating at 60 GHz [5] and Q-band high power amplifiers [6] are examples of MMICs based on GaAs pHEMTs that would benefit from a low phase noise oscillator. By integrating the Gunn diode on the same chip as the pHEMTs we can retain the advantages of a Gunn diode, such as superior phase noise, whilst using transistor gain to increase the oscillation power. Clearly, opportunities to develop more sophisticated hybrid device MMICs could be possible.

This work investigates the implementation of planar Gunn diodes and the pHEMTs on the same substrate for the future fabrication of high-power, high-frequency MMIC oscillators. Several examples of transistors integrated with other active devices have been demonstrated in the past like the implementation of HEMTs with resonant tunneling diodes (RTDs) [7] and p–i–n photodiodes [8].

Two different approaches are presented for the implementation of the planar Gunn diode and the pHEMT on the same substrate. Initially, the first technique is described in detail where the combined wafer consists of two groups of active layers that were independently optimized for the individual implementation of the two devices. A buffer layer is used for the isolation of the two devices. In another approach, a single wafer designed for the realization of GaAs-based pHEMTs was used for the implementation of both devices. In this technique a compromise has been conducted since the layer structure was not designed for the implementation of Gunn diodes. The latter approach demonstrated the first successful implementation of both devices on the same substrate for the first time, as presented in [9]. A 70 nm T-gate technology was incorporated for the optimization of the DC and the small-signal

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characteristics of the transistor. In the next sections, the fabrication procedures and the characterisation techniques performed for both approaches are described in detail.

2. The combined wafer approach

2.1. Wafer structure

The design of the combined wafer consists of two groups of active layers separated by a thick buffer of GaAs. Initially, the active layers of the Gunn diode were grown on a 620 μm thick GaAs substrate, using molecular beam epitaxy (MBE). The layer structure selected in this design for the realisation of the diode includes two GaAs channel layers that contribute mutually to the current conduction, sandwiched by 2 delta-doping layers each, as presented in [10]. Only the cap layer of the current design has been amended, where the graded GaAs/InGaAs structure has been replaced by highly-doped GaAs. This modification is required in order to avoid a lattice mismatch appearing between the top InGaAs surface with high Indium content and the GaAs buffer grown on top. In addition, the thickness of the cap layer is increased to 150 nm, providing an error margin while etching the top layers.

A thin layer of 5 nm lattice matched AlGaAs is deposited between the Gunn cap layer and the GaAs buffer layer. This performs as an etch-stop layer providing high accuracy while reaching the top of the Gunn structure, removing the pHEMT layers and the buffer. As described above, a GaAs buffer is grown after the Gunn layers where the thickness of the layer is equal to 1.1 μm ensuring electrical isolation between the two devices. The pHEMT layer structure, similar to the one presented in [11], is grown on the top of the buffer completing the growing procedure. The detailed layer structure of the combined wafer is presented in Table 1. The procedure of reaching the Gunn layers and the fabrication of the diode, are described in detail in the next section.

Table 1
The detailed layer structure of the combined wafer.

Material	Doping level	Thickness (nm)	Description
pHEMT layers			
GaAs	4×10^{18} cm^{-3}	30	Cap
$Al_{0.3}Ga_{0.7}As$		5	Etch stop
GaAs		2.5	Oxidisation stop
$Al_{0.3}Ga_{0.7}As$		7	Barrier
GaAs		2 ML	
Si delta doping	7×10^{12} cm^{-2}		
GaAs		3 ML	
$Al_{0.3}Ga_{0.7}As$		5	Spacer
$In_{0.2}Ga_{0.8}As$		10	Channel
GaAs		50	Buffer
Super lattice		5 periods	
GaAs		400	
Super lattice		50 periods	
GaAs		1100	pHEMT-Gunn isolation
$Al_{0.8}Ga_{0.2}As$		5	Etch stop reaching Gunn
Gunn layers			
GaAs	3.5×10^{18} cm^{-3}	150	Cap
$Al_{0.8}Ga_{0.2}As$		5	Etch stop
GaAs	3.5×10^{18} cm^{-3}	15	Gunn surface
$Al_{0.22}Ga_{0.78}As$		10	
Si delta doping	8×10^{11} cm^{-2}		
$Al_{0.22}Ga_{0.78}As$		10	
GaAs		50	Channel
$Al_{0.22}Ga_{0.78}As$		10	
Si delta doping	8×10^{11} cm^{-2}		
$Al_{0.22}Ga_{0.78}As$		10	
$Al_{0.22}Ga_{0.78}As$		10	
Si delta doping	8×10^{11} cm^{-2}		
$Al_{0.22}Ga_{0.78}As$		10	
GaAs		50	Channel
$Al_{0.22}Ga_{0.78}As$		10	
Si delta doping	8×10^{11} cm^{-2}		
$Al_{0.22}Ga_{0.78}As$		10	
GaAs		620 μm	

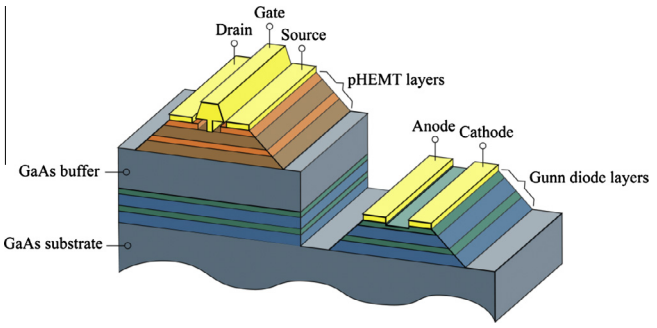

Fig. 1. The general layer structure of the combined wafer approach (not to scale).

2.2. Reaching the Gunn diode surface

A dry-etching procedure was followed for removing the pHEMT and buffer layers to access the Gunn layers (see Fig. 1). Dry etch was chosen instead of wet etch because of higher uniformity [12]. A hydrogen silsesquioxane (HSQ) negative electron beam resist was chosen for this step. The HSQ layer was initially spun at 6 k rpm and then baked at 90 °C for 15 min. The areas that are to remain for the protection of the transistor layers are exposed to the electron beam and the complementary windows are opened after the development of the HSQ. Electron beam lithography (EBL) has been used exclusively in this work using a Vistec Microsystems VB6 vector beam exposure tool.

The transistor and the buffer layers were then etched, using a reactive ion etching (RIE) technique with a silicon-tetrachloride ($SiCl_4$) gas environment. A test run was conducted prior to the actual fabrication, where an interferometer was used for the complete monitoring of the layer structure. In this step, the whole layer stack was removed reaching the semi-insulating GaAs substrate. The interferometer response that resulted from the test run is depicted in Fig. 2 with the pHEMT, buffer, Gunn and substrate areas highlighted. The same test procedure was performed three more times. The total etching time was different between the tests due to the varying condition of the RIE chamber. However, the same sequence of maximums and minimums was observed demonstrating the repeatability of the process.

For the fabrication of the actual Gunn diodes, the monitored dry-etching process was stopped before reaching the Gunn layers, leaving an error margin after the interruption of the etching. A wet-etching treatment was applied afterwards in steps of 30 s for reaching the AlGaAs etch stop layer. A 3:1 – $C_6H_8O_7$:H_2O_2 citric acid solution was used in this procedure, where the successful end of the etch stop layer was examined using a Dektak profilometer. Finally, a 10:1 buffered hydrofluoric acid (HF) solution was applied for 30 s for the removal of the AlGaAs layer.

2.3. Fabrication of planar Gunn diode

After removal of the top layers it was possible to fabricate the Gunn diode. The first lithographic step was the definition of the