Solid-State Electronics 83 (2013) 10–17

Contents lists available at SciVerse ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

Mushroom-free selective epitaxial growth of Si, SiGe and SiGe:B raised sources and drains

J.M. Hartmann [a,*], V. Benevent [a], J.P. Barnes [a], M. Veillerot [a], D. Lafond [a], J.F. Damlencourt [a], S. Morvan [a], B. Prévitali [a], F. Andrieu [a], N. Loubet [b], D. Dutartre [b]

[a] CEA, LETI, Minatec Campus, 17, Avenue des Martyrs, 38054 Grenoble Cedex 9, France
[b] STMicroelectronics, 850 Rue Jean Monnet, 38926 Crolles Cedex, France

ARTICLE INFO

Article history:
Available online 11 March 2013

Keywords:
Reduced Pressure – Chemical Vapour Deposition
Mushrooms-free Si and SiGe:B raised sources and drains
MOSFETs

ABSTRACT

We have evaluated various Cyclic Selective Epitaxial Growth/Etch (CSEGE) processes in order to grow "mushroom-free" Si and SiGe:B Raised Sources and Drains (RSDs) on each side of ultra-short gate length Extra-Thin Silicon-On-Insulator (ET-SOI) transistors. The 750 °C, 20 Torr Si CSEGE process we have developed (5 chlorinated growth steps with four HCl etch steps in-between) yielded excellent crystalline quality, typically 18 nm thick Si RSDs. Growth was conformal along the Si_3N_4 sidewall spacers, without any poly-Si mushrooms on top of unprotected gates. We have then evaluated on blanket 300 mm Si(001) wafers the feasibility of a 650 °C, 20 Torr SiGe:B CSEGE process (5 chlorinated growth steps with four HCl etch steps in-between, as for Si). As expected, the deposited thickness decreased as the total HCl etch time increased. This came hands in hands with unforeseen (i) decrease of the mean Ge concentration (from 30% down to 26%) and (ii) increase of the substitutional B concentration (from 2×10^{20} cm^{-3} up to 3×10^{20} cm^{-3}). They were due to fluctuations of the Ge concentration and of the atomic B concentration [B] in such layers (drop of the Ge% and increase of [B] at etch step locations). Such blanket layers were a bit rougher than layers grown using a single epitaxy step, but nevertheless of excellent crystalline quality. Transposition of our CSEGE process on patterned ET-SOI wafers did not yield the expected results. HCl etch steps indeed helped in partly or totally removing the poly-SiGe:B mushrooms on top of the gates. This was however at the expense of the crystalline quality and 2D nature of the ~45 nm thick $Si_{0.7}Ge_{0.3}$:B recessed sources and drains selectively grown on each side of the imperfectly protected poly-Si gates. The only solution we have so far identified that yields a lesser amount of mushrooms while preserving the quality of the S/D is to increase the HCl flow during growth steps.

1. Introduction

In situ doped recessed and raised sources and drains are extensively used nowadays in mainstream production in order to boost the performances of sub 100 nm gate length devices. Tens to roughly 100 nm thick embedded SiGe:B Sources and Drains (S/Ds) enable, thanks to (i) the uniaxial compressive strain in the Si channel injected by the compressively-strained SiGe layers nearby [1–4] and (ii) the low contact resistance provided by high B doping levels (a few 10^{20} cm^{-3}, typically), to significantly increase the electrical performances of p-type Metal Oxide Semiconductor Field Effect Transistors (MOSFETs). The benefits of using SiGe:B embedded SDs. were conclusively demonstrated for p-MOSFETs built on top of bulk Si(001) [5–10], bulk Si(011) [11], partially-depleted, tensily-strained Silicon-On-Insulator (SOI) [12,13], fully-depleted, Extra-Thin (ET)-SOI [14,15] substrates etc. Superior electrical performances were recently achieved thanks to facetted SiGe:B raised SDs. grown on each side of ET-SOI p-MOSFETs [16,17]. The Ge concentration in the SiGe:B embedded and raised S/Ds. has increased over time, from ~17% in 65 nm technology node devices (in 2003) to ~30–40% in current 28 nm technology node transistors [9].

The Selective Epitaxial Growth (SEG) of such SiGe:B embedded or raised SDs. is typically conducted at low temperature and low pressure with dichlorosilane + germane + diborane + hydrochloric acid [18–20]. Such a heavily chlorinated chemistry is indeed mandatory in order to be selective not only versus SiO_2 (i.e. the isolation in-between individual transistors) but also versus Si_3N_4 (the sidewall spacers of MOS transistors)). Low growth temperatures (in-between 600 °C and 650 °C, typically) are definitely advised in order to avoid any elastic relaxation of the compressive strain stored in rather high Ge concentration SiGe layers through the formation of surface undulations [21]. Finally, low pressures (20 Torr in the present case) help on patterned wafers in (i) obtaining full selectivity versus dielectric materials (such as SiO_2 or Si_3N_4) and (ii) minimizing the so-called loading effects (i.e. the definite

* Corresponding author. Tel.: +33 04 38 78 95 24; fax: +33 04 38 78 06 24.
E-mail address: jean-michel.hartmann@cea.fr (J.M. Hartmann).

0038-1101/$ - see front matter © 2013 Elsevier Ltd. All rights reserved.
http://dx.doi.org/10.1016/j.sse.2013.01.033

growth rate increase and the slight Ge content increase occurring when switching from blanket to patterned wafers and (on patterned wafers) when moving from densely packed, large Si windows to small, isolated Si windows) [18,20–22].

In some device integration schemes, however, the top of the gates is either not protected or imperfectly protected by a hard mask (for instance SiO_2). This can be a major problem as poly-Si (in the case of Si RSDs) or poly-SiGe mushrooms will then grow using as "seeds" the poly-Si layers sitting on top of the gate stacks. Those over-flowing mushrooms will hamper ion implantation close to the gate and merge for dense devices such as Static Random Access Memory (SRAM) cells (leading then to major S/D thickness fluctuations). This problem was solved, at least for Si RSDs, thanks to Cyclic Selective Epitaxial Growth/Etch (CSEGE) processes, which consist in several repetitions of chlorinated growth steps (inherently selective versus dielectrics) and selective poly-Si etch steps (thanks to gaseous HCl) [23,24]. We will present in the following the various processes we use in the CEA-LETI 300 mm pilot line to grow "mushroom-free" Si RSDs on ET-SOI substrates. We will then detail the salient features of the process we have evaluated to obtain "mushroom-free" intrinsic SiGe and SiGe:B RSDs.

2. Experimental details

A 300 mm Epsilon 3200 Reduced Pressure – Chemical Vapour Deposition (RP-CVD) tool from ASM America was used to grow all the layers in this study, with the growth pressure kept at 20 Torr. The purified H_2 carrier gas flow, several tens of standard litres per minute, was not altered throughout the experiments. Pure dichlorosilane, germane and diborane diluted at respectively 10% and 2000 ppm in ultra-pure H_2 were used as Si, Ge and B precursors gases. Pure hydrochloric acid was used in order to boost selectivity and/or etch layers in CSEGE schemes. The thickness of the SiGe:B layers grown on slightly p-type doped 300 mm bulk Si(001) wafers was obtained from Fast Fourier Transforms of X-ray Reflectivity (XRR) profiles (acquired on a fully automated Jordan-Valley tool with a convergent incident X-ray beam and a 1024 pixel Charge-Coupled Display detector that samples the reflected beam over an ~3.5° range). Conventional Omega–2Theta scans around the (004) X-ray Diffraction (XRD) order were used to give another estimation of the SiGe:B layer thickness, to calculate the Ge concentration and to check that layers were fully strained and of high crystalline quality. A X'Pert Panalytical tool with a copper anticathode as the X-ray source (λ Kα_1 = 1.5406 Å), a 4 bounce symmetric Ge(220) Bartels' monochromator and wide slits in front of the detector was used for those XRD measurements. Time-of-Flight Secondary Ions Mass Spectrometry (ToF-SIMS) depth profiling of the Si, Ge, and B atoms present in our SiGe:B layers was carried out with an ToF SIMS V tool from ION TOF GmbH. Si and Ge quantification was performed using 500 eV Cs^+ primary ions and the extended Full Spectrum protocol detailed in Ref. [25]. B depth profiling was carried out using 500 eV O_2^+ primary ions. Spectroscopic ellipsometry measurements of dedicated 70 × 100 μm^2 area with a KLA Aleris tool enabled us to gain access to the Si or SiGe:B deposited thickness in the large windows of patterned ET-SOI wafers. Finally, top-view and cross-sectional Scanning Electron Microscopy (SEM) pictures of our Si and SiGe:B raised SDs. were acquired on a Hitachi CG4000 tool (that handles 300 mm wafers) and on a Hitachi SEM 5000 apparatus, respectively.

3. The various Si raised sources and drains SEG and CSEGE processes developed

The standard Si SEG process we have developed in 2004 to thicken the Sources and Drains regions of ET-SOI MOSFETs (and thus lower series resistance) consists in the following: an *ex situ* "HF-last" wet cleaning, an in situ H_2 bake at 650 °C for 2 min, a slow (2.5 °C/s) temperature ramping-up under H_2 from 650 °C up to 750 °C followed by Si SEG at 750 °C, 20 Torr thanks to SiH_2Cl_2 + HCl [26]. The Si growth rate in our 300 mm tool is typically 2.7 nm min^{-1} with the mass-flows used ($F(SiH_2Cl_2)/F(H_2)$ = 5.33×10^{-3} and $F(HCl)/F(H_2) = 1.11 \times 10^{-3}$). Such a process, which is fully selective versus SiO_2 (the isolation) and Si_3N_4 (the sidewall spacers), will lead to the formation of poly-Si mushrooms of top of unprotected or imperfectly protected gates, as shown in Fig. 1 for 23 nm Si RSDs (coming from Ref. [24]).

In order to solve this problem, we have developed two "mushroom-free" processes. The first one, which is rather straightforward, consists in the SEG at 750 °C, 20 Torr with the same flow of SiH_2Cl_2 and HCl of ~22.5 nm of Si, followed by the selective removal at 700 °C, atmospheric pressure with a high HCl mass-flow ($F(HCl)/F(H_2)$ = 0.444) of the poly-Si mushroom sitting on top of the gate. ~4.5 nm of mono-crystalline Si is removed in the SD regions during this 2 min etch, yielding in the end the 18 nm thick Si RSDs aimed for. This process is very handy when thickening the S/D regions of Si nanowires (NWs). The access regions of NWs are indeed significantly thickened then slightly trimmed down as the poly-Si mushrooms of top of the gate are removed. By contrast, the use of CSEGE will lead to the breaking-up of the still narrow NWs during the first few etch steps. Thickening the Si S/D regions then removing the poly-Si mushrooms in two steps only has however some drawbacks as well, notably in dense structures such as SRAM cells. The overflowing mushrooms on top of nearby gates will indeed merge during growth, leading to major S/D thickness fluctuations prior to poly-Si mushroom selective etching.

The second process we have developed is based on a 750 °C, 20 Torr CSEGE approach. It consists in 5 SiH_2Cl_2 + HCl growth steps separated from one another by 4 smaller HCl mass-flow ($F(HCl)/$

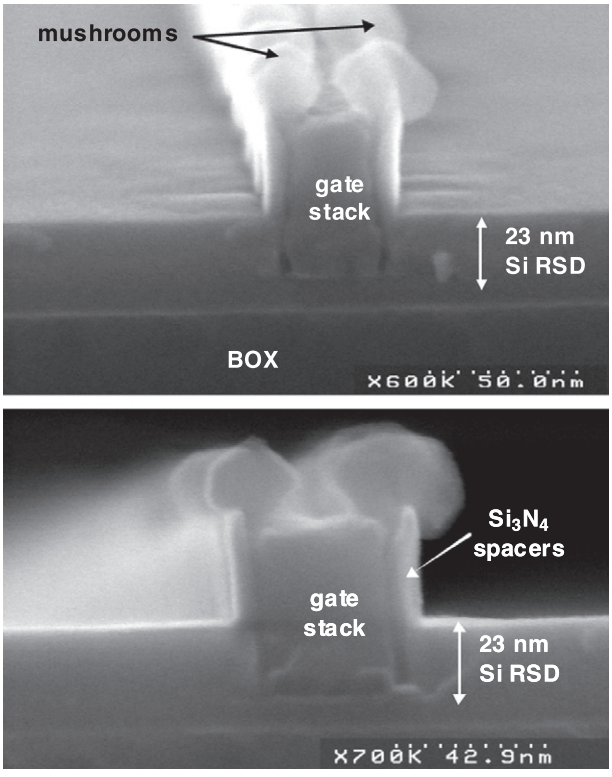

Fig. 1. 3D and cross-sectional SEM pictures of a short gate length ET-SOI MOSFET after the 750 °C, 20 Torr selective epitaxial growth of 23 nm thick Si raised sources and drains.