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Analysis of trap-assisted tunneling in vertical Si homo-junction and SiGe hetero-junction Tunnel-FETs

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ABSTRACT

This paper reports on the integration of vertical nTunnel FETs (TFETs) with SiGe hetero-junction and analyzes the presence of trap-assisted tunneling impacting the device behavior. Temperature measurements are used to distinguish the band-to-band tunneling (BTBT) from the trap-assisted tunneling (TAT). It is shown that TAT degrades the onset characteristic and the subthreshold swing of the devices. TCAD simulations are in good agreement with experimental data for a germanium content up to 44%, when including non-local TAT model and properly tuning the model's parameters. Simulations also suggest that boosting the BTBT component, for example by further bandgap decrease (Ge source), or by other means should be beneficial in lowering the impact of trap-assisted tunneling, provided that the material defectivity does not worsen.

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1. Introduction

Recently, the TFET has attracted much attention as a promising candidate for ultra low power applications due to its steeper switching behavior than MOSFETs (SS < 60 mV/dec) [1,2]. However, the reported performance of fabricated silicon TFETs remains poor compared to that of MOSFETs. The on currents are too low (0.1–1 μA/μm range) due to the large silicon bandgap, and the reported average subthreshold swings are typically in the 100–150 mV/dec range. Several solutions have been identified to boost the tunneling properties of TFETS, such as (1) improved electrostatics (device configuration, body thickness, and EOT) [3,4], (2) low bandgap at the source (use of materials such as Ge or III–V and strain) [5,6], and (3) junction optimization (doping level and profile) [7]. TFETs fabricated using some of these features have shown improved performance [8–14]. In this prospect, vertical TFETs [15,16] are very attractive as their gate-all-around configuration combined with small nanowire diameters provides the best gate electrostatic control on the channel. Moreover, hetero-structures can easily be implemented using vertical epitaxial growth [17]. In addition, junction abruptness obtained by epitaxy is typically superior to the one obtained by ion implantation. In this paper, we report on the integration and electrical performance of vertical Si homo-junction and SiGe source hetero-junction TFETs. The presence of trap-assisted tunneling is analyzed in details through temperature characterization and TCAD simulations.

2. Device fabrication

The devices are fabricated using a vertical process flow similar to the one reported in [18,19] for Si vertical TFETs. In the case of the SiGe hetero-TFETs, the channel and top source region are formed by blanket epitaxial growth of an undoped silicon layer (channel) followed by an in situ boron-doped $Si_{1-x}Ge_x$ layer ($x = 0.27$) (source), using an ASM Epsilon^{TM} 200. Devices with a higher Ge concentration are obtained by inserting a thin 6 nm intermediate B-doped $Si_{0.56}Ge_{0.44}$ layer (pocket) in between the channel and the B-$Si_{0.73}Ge_{0.27}$ source. The thickness of the B-$Si_{0.56}Ge_{0.44}$ layer has to remain lower than its critical thickness to avoid relaxation [20] and defects formation at the channel interface. The undoped silicon channel and B-doped $Si_{1-x}Ge_x$ growths are performed by chemical vapor deposition (CVD) at 650 °C and 450 °C, respectively, following a pre-bake at 1050 °C. The pillars are then patterned using a 193 nm lithography and an oxide hardmask. Resist trimming techniques are used to achieve ~400 nm tall nanowires with diameters (d_{NW}) ranging between 70 nm and 200 nm. A 150 nm-thick bottom oxide layer is implemented using a high density plasma (HDP) oxide deposition followed by chemical–mechanical polishing (CMP) and oxide wet etch-back. This bottom isolation serves to isolate the gate from the substrate and to create an underlap of the gate with the drain reducing the tunneling at the drain side and suppressing the ambipolar effect [21]. A gate

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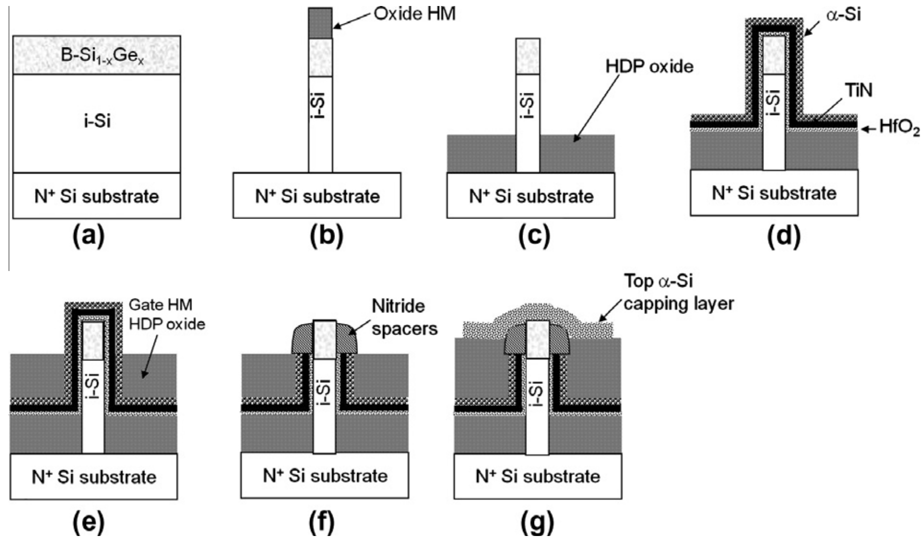

Fig. 1. Schematic description of the process flow of the vertical hetero-Tunnel FET.

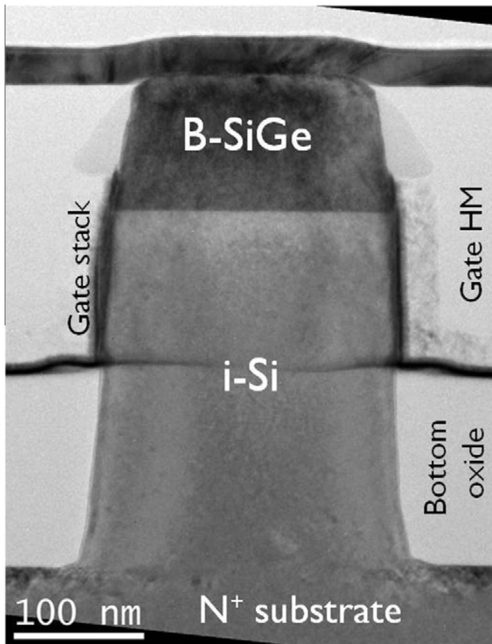

Fig. 2. TEM cross-section of a vertical 200 nm-diameter nTFET with a B-doped $Si_{0.73}Ge_{0.27}$ source.

stack of 3 nm atomic layer deposition (ALD) HfO_2, 5 nm plasma-enhanced ALD TiN and 30 nm low pressure chemical vapor deposition (LPCVD) amorphous Si is deposited on top of a 1 nm interfacial silicon oxide. A second HDP oxide is then deposited followed by CMP and oxide etch-back to form the gate hardmask. This gate hardmask defines the amount of overlap between the gate and the source in the device. Another lithography step followed by oxide etch is then used to expose part of the gate located on top of the bottom isolation. The exposed gate stack is then removed by dry etch. This allows for top source contacting as well gate separation between different devices. The top source contact is isolated from the gate by a nitride spacer together with a third HDP oxide. After CMP of the third HDP oxide, the source contact is formed by the deposition of an intrinsic amorphous Si layer which, after patterning, connects multiple nanowires together. After patterning of the source contact layer, the oxide covering the gate contact pads and routing is removed. Contrary to [18], the source contact layer is not implanted and annealed but fully silicided with nickel, together with the exposed gate contact pads and routing. This avoids a dopant activation step and maintains the thermal budget during processing below 700 °C, resulting in very low dopants diffusion. The devices feature ~150 nm physical gate length with 30 nm gate-source overlap. The schematic process flow and a TEM cross-section of the final vertical nTFET are illustrated in Figs. 1 and 2, respectively. The 1D vertical doping profile at the

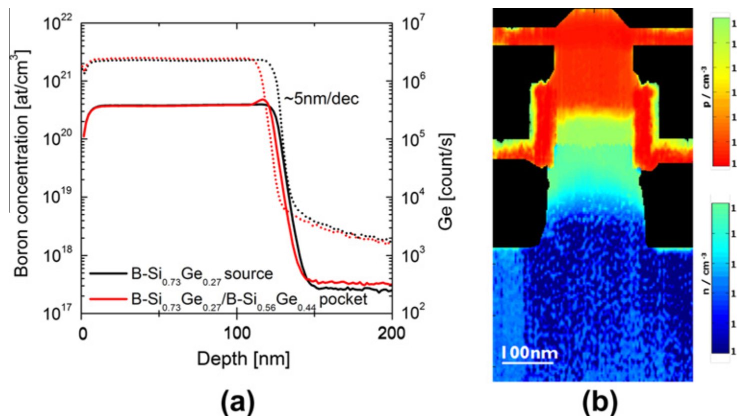

Fig. 3. (a) Boron profile at the top B-$Si_{1-x}Ge_x$/i-Si junction (dotted line, left y-axis) and Ge count (solid line, right y-axis) after growth and processing from SIMS analysis and (b) quantitative 2D carrier distribution obtained by SSRM in a 200 nm nanowire B-$Si_{0.73}Ge_{0.27}$/B-$Si_{0.56}Ge_{0.44}$-source TFET.

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