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Controlled on-chip heat transfer for directed heating and temperature reduction

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ABSTRACT

Accurate thermal modeling is critical to address the heating-related problems in integrated circuits, as well as to ensure as-designed operation or to obtain performance predictions in a range of different operating conditions. We present our experimental and theoretical work on modeling thermal behavior in integrated circuits (ICs) at the resolution of single material layers. Through measurements and simulations we find that lateral metal interconnect networks have minimal effect on directing heat flow in bulk technologies, but may be more influential in SOI systems. Thermal via structures are effective for temperature reduction in either case. With this approach we are able to contribute to the IC design process by suggesting metal layout features for cooling and controlled heating.

1. Introduction

We investigate the effects of metal layout features, such as via structures and interconnects, on temperature distribution and reduction in integrated circuits (ICs). We study the use of these features in on-chip controlled and directed heating. Through measurements and simulations, the latter performed at the resolution of single material layers, we explore and characterize the effects of metal interconnect networks on directing heat flow in bulk and silicon-on-insulator technologies. We then use these studies to suggest layout schemes for governing heat flow for controlled heating and cooling of integrated circuits.

Several factors motivate research into thermal effects in the IC physical system. For example, modern microprocessor circuits often exhibit very high power densities, causing prohibitively high operating temperatures. At the other extreme, electronics for cryogenics are finding high demand in space applications and might require circuit heating for proper operation. Such factors call for integrating detailed thermal effect simulations into IC design flow.

Heating problems from higher on- and off-state (leakage) power are a bottleneck in the development of more tightly integrated systems, with high device densities, clock frequencies, and supply voltage scaling limitations [1–5]. Silicon-on-insulator (SOI) and three-dimensional integration (3DI) technologies exacerbate the problem, since their physical structures include more insulating oxide layers between the heat-generating active layer and the ambient as compared to planar bulk technologies [6]. Thermal management is necessary to prevent excessive IC heating. Hardware- and software-based and hybrid management approaches have been proposed for digital [7,8] and analog [9,10] circuits. Schemes to temporarily reduce power consumption, to compensate for the electrical effects of temperature change, and to carry away excess heat have been considered. For the latter, dedicated metal-level layout schemes and vertical vias in planar and 3-D circuits have been suggested [3,11–15]. Here we evaluate this suggestion in further detail using experimental data and simulations.

Built-in IC features to establish a specified operating temperature could also be useful, for instance in extreme-environment applications, like electronics designed for cryogenic temperatures. Such circuits could use controlled or directed local heating, where a chip or a chip region is warmed to a preset temperature without wasting power by externally heating the full system [16]. Temperature control on the chip scale and intra-chip regions also finds applications in biological sciences, for instance in processes such as polymerase chain reaction (PCR) thermal cycling [17], or hybridization/dehybridization enhancement by temperature change in DNA detection, especially in setups where a given region of a detector chip is reserved for a single target sequence [18,19].

Accurate thermal modeling over the chip geometry is necessary during design, since device properties and performance depend on operating temperature. Devices dissipating heat in operation affect their own thermal environment in turn. Depending on the

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operation, physical design, and the ambient conditions, this effect might lead to a self-determined operation temperature [16] or an uncontrollable thermal runaway. Moreover, devices designed for identical performance might not match as intended if placed in different-temperature chip regions. The designer would benefit from the ability to estimate the temperature distribution in an operating chip. Thus, integrating heating and cooling effects into the chip design flow is desirable.

To study, characterize and develop design techniques utilizing on-chip heat transfer, we expanded an in-house coupled thermal and electrical chip performance simulator. We have also designed specially-tailored integrated circuits for measuring on-chip temperature profiles and had them fabricated through the MOSIS fabrication service [20]. By carefully calibrating and validating the custom thermal simulator with the measurements from on-chip temperature meters, we developed a tool that allows for the quantitative analysis and prediction of heat flow in integrated circuits. We then use this tool to evaluate heat flow in bulk and SOI based circuits.

We find that lateral metal interconnect networks have minimal effect on directing heat flow in bulk technologies, but may be more influential on silicon-on-insulator (SOI) systems. In both technologies, thermal via structures in various configurations effectively reduce heating caused by on-chip sources. We also investigate methods to design and evaluate layout features for controlled and directed on-chip heating. For example, we present metal structures that both guide and/or confine heat flow to establish a temperature profile that could be useful for circuit performance. More specifically, we implement heat frames and fences that confine temperature rise due to on-chip heat sources, to a desired chip area, and facilitate heat flow to other regions. We are thus presenting a flexible method to explore on-chip thermal effects as well as to incorporate thermal design into the chip design process.

This paper starts with an outline of our modeling methodology and thermal mesh creation. We next present two integrated circuits designed and fabricated to verify and calibrate our simulator, and also to investigate the effects of the planar interconnect mesh on the chip temperature profile. After the experimental and calibrated simulation results, we demonstrate that while the substrate dominates heat transfer in bulk technologies, in SOI technologies the metal layer layouts more strongly affect on-chip temperature distributions. We continue with displays of the use of thermal via frames and fences for cooling and controlled heating.

2. Modeling method

This section outlines the methodology of our in-house integrated circuit thermal modeling/simulation program. More details on this program, which we built upon for this present work, can be found in [3,4,16]. The algorithm is based on the creation of a thermal network, which couples individual device performances to the device and chip heating, and calculating a self-consistent solution to this network. By modeling device Joule heating, heat storage and transmission as thermal current sources, capacitors and resistors, respectively, a thermal network can be created at the chip level at the resolution of a single device. Then the heat conduction equation, given below, can be discretized and converted to a set of Kirchhoff's Current Law (KCL) equations, solved over this thermal network. Such an example network at steady state can be seen in Fig. 1. At the top of Fig. 1, we show a chip section with 3×3 devices (M_{ij}, where $i,j = 1,2,3$). Each device generates heat, which is represented by the current sources. We then insert these sources into the thermal resistor network and calculate the nodal temperatures. Later, we update the heat generated by each device according to its temperature. This method has been expanded for the

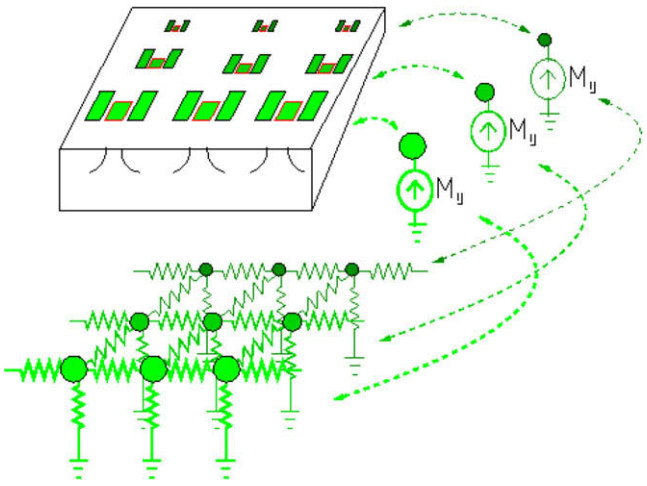

Fig. 1. A chip-wide steady state thermal network model. Top: A chip section with 3×3 devices. Right: Each device generates heat, which is represented by a current source. Bottom: Devices are thermally coupled to their neighbors by an equivalent resistive network.

simulation of 3-D chip stacks: 2-D networks model each planar chip tier, and separate 2-D networks represent the oxide layers between the tier substrates, with vertical links connecting these networks [4] to form the final 3-D stack. This program can guide a designer towards layout schemes for temperature reduction, or for controlled and directional heating.

At the chip level, the temperature distribution at steady state is obtained by discretizing and solving the steady state version of the heat conduction equation:

$$\vec{\nabla} \cdot (\kappa(\vec{r})\vec{\nabla}T(\vec{r})) = -H(\vec{r}), \tag{1}$$

where T is the temperature, κ (W/m K) is the thermal conductivity and H (W/m^3) is the heat source density. In non-uniform structures, κ also depends on position $\vec{r}$; and in non-isotropic structures it can be represented as a tensor. The term $-\kappa(\vec{r})\vec{\nabla}T$ describes the heat flux vector. Eq. (1) is discretized to be solved over the equivalent thermal network described above. Further details about the construction of this network layer-by-layer follow.

The thermal distribution characteristics of different IC material layers have previously been merged into effectively averaged characteristics for simulation [3,4]. Thermal resistive elements represent the averaged thermal attributes of the differential physical die volume surrounding the node. However, there are incentives to consider the individual geometries of each material layer when setting up the thermal network. For instance, polysilicon and metal layers include highly conductive directional features compared to their surrounding insulator layers. Thus, even though they occupy a small volume, they may need to be represented separately instead of being averaged out. Furthermore, not only the active devices in the substrate but also structures like resistors and inductors manufactured on other layers generate heat. It has also been suggested that in signal-dense applications, interconnects themselves are responsible for a portion of heat generation with non-negligible thermal effects [21,22]. Finally, in the case where interconnect layers and vias are designed to aid cooling, their particular effects on heat conduction need to be modeled at a resolution which considers material layers individually.

Therefore in this work we refine our approach and account for the layout at each material layer. We create a 3-D mesh even for planar chips, with nodes placed in every individual layer (e.g. going up from the substrate: substrate, oxide, polysilicon, oxide, metal, oxide, metal, oxide for a single-poly, two-metal process, as