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Impact of quantum effects on the short channel effects of III–V nMOSFETs in weak and strong inversion regimes

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ABSTRACT

This paper investigates the impact of quantum effects on the increase of short channel effects in III–V MOSFETs. First of all, contrary to the results obtained by other groups [1,2], quantum confinement has been found to play no role on the short channel effects occurring in the subthreshold regime. In this regime, the main origin of the increase of SCEs is simply due to the higher dielectric constant of III–V semiconductors. However, in strong inversion regime, the increase of the electrical equivalent oxide thickness due to quantum confinement is shown to have a detrimental impact on the drain induced barrier lowering. These results further confirm that III–V technologies will require innovative devices like ultra-thin films or multi-gate structures to ensure a better control short channel effects.

1. Introduction

The replacement of silicon as channel material by III–V semiconductors has emerged as a realistic option for the end of the roadmap of CMOS [3]. Indeed, these materials present greatly improved transport properties with respect to unstrained or strained silicon [4]. Many experimental results have already been published and recently, Radosavljevic et al. [5] have presented a tri-gate III–V structure showing promising performances, especially regarding the control of short channel effects (SCEs) control.

Simulations and experimental results have shown that III–V technologies are subject to enhanced short channel effects, including larger V_t-roll Off, larger drain induced barrier lowering and subthreshold slope than the silicon devices [5–8], which might compromise their use for the end of the roadmap of CMOS devices [9]. In particular references [6,7] have shown by numerical simulation and analytical modeling that the subthreshold slopes of Ge and III–V MOSFET were larger than in Si, and [8] has demonstrated that $In_{0.7}Ga_{0.3}As$ Quantum Well FETs present poor scalability for the same reason.

In addition to the increased SCEs, it has been shown by the mean of simulation that quantum confinement in III–V channel is enhanced [10,11]. Indeed, due to the smaller effective masses and hence the smaller the density of states (DOS) of these semiconductors, a larger degradation of the gate coupling with the channel is expected with respect to silicon channel [12]. This effect is shown to result in an increased electrical Equivalent Oxide Thickness (EOT) with respect to the physical oxide thickness, phenomenon also called dark space [10–13].

Recently published results [1,2] have stated that they could impact the short channel effects in the subthreshold regime. However, these results are questionable as the approach used in these works consists in comparing a classical simulator, an analytical model based on Poisson–Schrödinger fitting and quantum corrected TCAD simulation. These codes comparisons are known to show some significant divergences and should be carried out with care, as done in reference [14] for different quantum confinement codes or in [15] for different codes of transport in nanoscale nMOSFET.

Moreover, SCEs have been shown to have a detrimental impact on inverter performances in the strong inversion regime. Indeed, it has been shown in [16,17] that the SCEs in strong inversion regime, and especially the non saturation of the drain current caused by the Drain Induced Barrier Lowering (DIBL) could severely degrade the delay and propagation time of inverter and ring oscillator. Therefore, a comprehensive evaluation of the impact of SCEs in III–Vs should not be limited to the subthreshold regime only, as carried out in [6–8], but should also include strong inversion. In this regime however, the impact of quantization on the inversion charge is no longer negligible, which raises the question of role of quantum effect on the DIBL in strong inversion.

Two questions hence still remain open: 1/Do quantum effects impact the short channel effects in the subthreshold regime? 2/Do quantum effects impact the DIBL in the strong inversion regime? Therefore, Section 3 of this work will investigate of the SCEs in subthreshold regime, with and without quantum effects. Section 4 will then presents the role quantum effects on the DIBL in strong inversion regime.

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2. Short channel effects in subthreshold regime

Essentially seen as a source of off state current degradation, short channel effects are usually investigated in subthreshold regime. Fig. 1 summaries the modifications of the I_d–V_g and I_d–V_d characteristics of a MOSFET induced by of short channel effects: they are characterized, in subthreshold and ohmic regime, by a smaller threshold voltage (V_t) for shorter length, an increased subthreshold slope (in mV/dec), and a decreased V_t at high V_d due to DIBL (in mV/V). In this section, only the DIBL and the subthreshold slope will be used as figure of merit of SCEs, as they are the main cause of leakage increase.

To investigate the potential effect of quantum confinement on short channel effects, several previous works have compared the results obtained using classical simulator with results obtained with an analytical model and quantum corrected TCAD simulator [1,2]. However, this simple approach is questionable, as these different tool, not only differ from the physics, but they also use very different boundary conditions or mesh. This kind of issue has been investigated in systematic code comparisons like in Refs. [14,15], which shows that difference can arise from code using the same approach.

Therefore, to avoid this issue, the results presented in this section have been obtained using the same tool, i.e. the NanoMOS [18,19] simulator suit, which self consistently solves the Poisson–Schrödinger (PS) equations, along the channel, with different transport models. Indeed, although NanoMOS being better known for its Non Equilibrium Green Function (NEFG) transport model, it also include a Ballistic Transport Model (BTM) model and a Drift Diffusion (DD) model, which are all self consistently solved with the PS equations [18]. The NEFG model in NanoMOS is a ballistic transport model which account for all source-drain tunneling component, and in particular the subthreshold source-to-drain tunneling, which have been shown to be significant for ultra short channel (<15 nm) III–V nMOSFET [20,21]. The BTM is a ballistic transport model which neglects the source-drain tunneling component of the drain current. The DD model available in NanoMOS differs from conventional drift diffusion model as the charge is rigorously calculated using a Poisson–Schrödinger solver.

To study the impact of quantum effect on subthreshold SCEs, NanoMOS simulations have been performed changing the effective masses, in order to artificially modify the strength of quantization by 1/increasing the subband splitting through the decrease of the confinement effective mass and 2/reducing the DOS in the conduction band through the decrease of the density of state effective mass [22]. These two effects, and in particular the DOS reduction, will therefore highlight any dependency of SCEs with quantum confinement and especially of the dark space [10,11,13].

The devices considered in this section are template double gate MOSFETs with a 5 nm film thickness, 1 nm EOT and 10 nm source/drain length. To avoid any confusion with the increase of subthreshold slope due to the SCEs, source-to-drain tunneling has been kby using the Dirft–Diffusion model. Three gate lengths (L_g) have been considered: 10, 15 and 20 nm and, as explained, the density of state effective mass of the channel material has been varied from $0.05m_0$ to $1m_0$. The obtained DIBL and subthreshold slope are shown in Fig. 2.

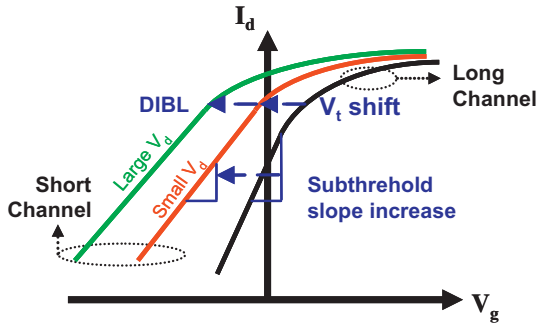

Fig. 1. Schematic representing the impact of short channel effects on the I_d–V_g characteristics of an nMOSFET.

Contrary to [1,2], who argued that quantization does affect the SCEs in subthreshold regime, the results obtained here with NanoMOS do not show any modification of the DIBL or the subthreshold slope when the density of states effective mass is changed. These results have also been obtained when considering different values of the confinement effective mass, which mainly influence the value of the long channel threshold voltage, but do not modify the subthreshold slope or the DIBL. Therefore, neither the subband splitting induced by the reduction of the confinement effective mass, nor the increase of dark space induced by reduced DOS effective mass modifies the SCEs. In weak inversion regime, the channel potential is hence still mostly controlled by geometry, the built-in potentials and the depletion charges.

Classical simulation can therefore correctly capture SCEs. To illustrate further the impact of the channel material parameters on the short channel effects, the double gate devices have been simulated with varying energy bandgaps and varying dielectric constant, by self-consistently computing the Poisson and Drift–Diffusion equations with a 2D partial differential equations solver. These double gate devices feature a film thickness (t_{sc}) of 5 nm and an EOT of 1 nm. The same three gate lengths (10, 15 and 20 nm) have been simulated.

The DIBL and Subthreshold slope have been firstly extracted for varying values of bandgap, as the channel potential profile depends on the built-in potential between the source/drain and channel pn junctions, and hence on E_g [23,24]. These results are shown in Fig. 3 and compared with the results obtained from the analytical model presented in [7]. It can be seen from Fig. 3 that the subthreshold slope of the double gate is independent of the bandgap value of the semiconductor. Results obtained by simulation and the model have been found in agreement, without fitting procedures. DIBL however seems to be a weak function of the bandgap, mostly in devices featuring large SCEs (e.g. L_g = 10 nm and t_{sc} = 5 nm). The discrepancy between the model and the simulations becomes larger for values of L_g/t_{sc} smaller than 2, which correspond to the limit of validity of the model [7].

Similar simulations have been performed for varying dielectric constants of the channel material. The DIBL and subthreshold slope

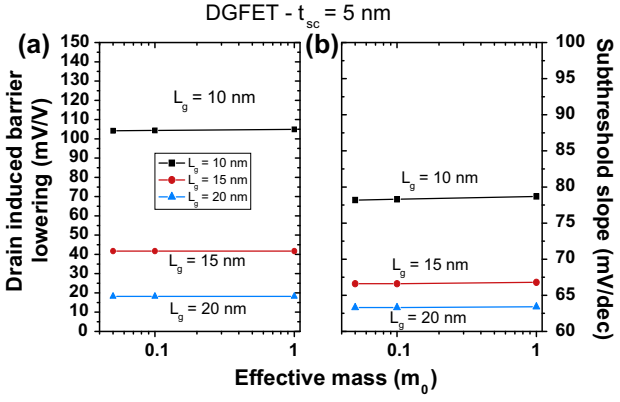

Fig. 2. Drain induced barrier lowering (a) and subthreshold slope (b) as a function of the density of state effective mass, obtained with NanoMOS in the drift–diffusion model, for three different gate length (L_g = 10, 15 and 20 nm) of double gate MOSFET featuring a channel thickness of 5 nm and an EOT of 1 nm.