Solid-State Electronics 88 (2013) 49–53

Contents lists available at SciVerse ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

Investigation of localized versus uniform strain as a performance booster in InAs Tunnel-FETs

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ARTICLE INFO

Article history:
Available online 5 June 2013

Keywords:
Tunnel FET
Nanowire
Strain
InAs
NEGF

ABSTRACT

We investigate the effect of spatially localized versus uniform strain on the performance of *n*-type InAs nanowire Tunnel FETs. To this purpose we make use of a simulator based on the NEGF formalism and employing an eight-band $\mathbf{k}\cdot\mathbf{p}$ Hamiltonian, describing the strain implicitly as a modification of the band-structure. Our results show that, when the uniform strain degrades the subthreshold slope because of an increased band-to-band-tunneling at the drain, a localized strain at the source side permits to obtain a better tradeoff between on-current and subthreshold slope than a uniform strain configuration.

1. Introduction

Tunnel-FETs are among the most promising electron devices that, by reducing the inverse subthreshold slope (SS) below 60 mV/dec at room temperature, may lead to digital integrated circuits operating at a supply voltage, V_{DD}, substantially lower than 0.5 V [1], as required by minimum energy circuit design methodologies [2]. Together with variability issues [2], arising from defects or spatial fluctuations [3], the main drawback of Tunnel-FETs with respect to standard MOSFETs is that they provide poor on currents (I_{on}) [4], so that improving the I_{on} while preserving small off currents (I_{off}) and SS values is probably the greatest challenge in the design of Tunnel-FETs [1]. To this aim several solutions have been investigated as the use of high-κ dielectrics, spacers and underlaps [5,6], of strain in Si, Ge and SiGe Tunnel-FETs [7,8], of broken and staggered bandgaps in III–V or II–VI materials [9,10] and of graphene based Tunnel-FETs [11]. Recently, it has been proposed that a relevant improvement in the performance of homo-junction InAs nanowire (NW) Tunnel-FETs can be obtained by using appropriate stress conditions [12,13]. In particular, it was shown that the biaxial tensile strain reduces the gap as well as the imaginary wave-vector in the energy gap of InAs, resulting in remarkable drain current improvements with a modest increase of the sub-threshold slope.

This paper investigates the potential advantages of a localized versus a uniform strain condition for the performance enhancement of *n*-type InAs NW Tunnel-FETs. To this purpose, we exploited a self-consistent three-dimensional (3-D) quantum transport simulator based on the non-equilibrium Green's function (NEGF) formalism and on the eight-band $\mathbf{k}\cdot\mathbf{p}$ Hamiltonian proposed in [14]. The numerical simulator, already presented in [12,13], has been extended to deal with strain conditions that vary along the transport direction. Our results show that, if the stress is mainly localized at the source, an improvement of the inverse subthreshold slope can be achieved with respect to the uniform strain with essentially no degradation of the I_{on} value. This can help to further enlarge the window of I_{off} and V_{DD} values where Tunnel FETs may outperform silicon MOSFETs.

2. Simulated devices

The gate-all-around (GAA), rectangular nanowire transistors studied in this work are sketched in Fig. 1, where x is the transport direction and carriers are confined in the y–z plane, with (x,y,z) forming the device coordinate system. All simulated devices are (100) nanowires, hence x, y and z are equivalent ⟨100⟩ directions.

When considering the InAs Tunnel-FETs, we studied both a symmetric device with the same doping concentration $N_S = N_D = 5 \times 10^{19}\ \mathrm{cm}^{-3}$ at source and drain and an asymmetric transistor with $N_S = 5 \times 10^{19}\ \mathrm{cm}^{-3}$ and $N_D = 10^{18}\ \mathrm{cm}^{-3}$. An abrupt junction between doped regions and channel has been used.

3. Transport and strain modeling

We performed quantum transport simulations based on the self-consistent solution of the 3-D Poisson and Schrödinger

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http://dx.doi.org/10.1016/j.sse.2013.04.005

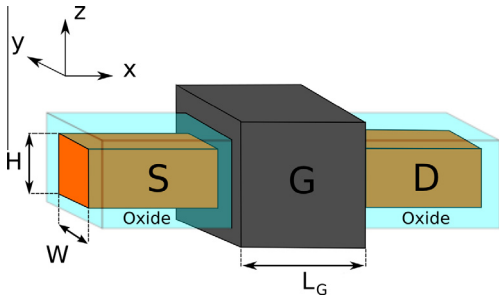

Fig. 1. Sketch of the simulated nanowire transistors. The device coordinates x, y and z are equivalent ⟨100⟩ directions.

equations within the NEGF formalism. The strained Si MOSFETs were modeled according to the effective mass approximation [15], whereas for InAs Tunnel-FETs we used a recently developed quantum transport simulator [12], which is based on the eight-band $\mathbf{k}\cdot\mathbf{p}$ Hamiltonian proposed in [14], that describes the valence and conduction bands at the Γ point and accounts for the spin–orbit interaction. The adoption of a more complex Hamiltonian to simulate InAs Tunnel-FETs was necessary to take into account electron tunneling from the valence to the conduction subbands. It has been recently argued that the spurious solutions of the differential operators obtained by introducing the quantization in the $\mathbf{k}\cdot\mathbf{p}$ Hamiltonians are mainly caused by the possible non-ellipticity of such operators [16]. To eliminate the spurious solutions in our $\mathbf{k}\cdot\mathbf{p}$ problem the parameter E_p controlling the mixing of valence and conduction bands was set to the value recommended in [16], which assures that the Hamiltonian operator is elliptic.

The discretization of the three-dimensional Hamiltonian in real-space (namely with the finite difference method) leads to a computationally intractable problem. We thus resorted to the theoretically equivalent *coupled* mode-space formulation [17,12]. Since carrier transport is determined only by modes with eigenenergies close to the bottom of the conduction band and to the top of the valence band, a very good approximation of the transport properties of our devices can be achieved with a finite number of modes. As already pointed out in [17] the calculation of the modes in each device section is still too much CPU and memory demanding with a standard finite difference discretization. Hence, to speed up the determination of modes, the 2-D Schrödinger equation was solved by using a basis of sine functions.

The mode-space retarded Green's function G^R_{MS}, lesser-than $G^<_{\mathrm{MS}}$ and greater-than $G^>_{\mathrm{MS}}$ Green's functions were then computed via a recursive algorithm based on the Dyson equation; the self-energies of the contacts were obtained with the iterative scheme of [18]. We typically used 50 modes in our simulations and verified that the results were practically insensitive to a further increase of the number of modes.

In case of non-zero phonon scattering the kinetic equations for the retarded and the lesser-than Green's functions are non-linearly coupled and need to be self-consistently solved. Here, the lesser-than self-energies for phonon scattering are expressed within the self-consistent Born approximation $\Sigma^{<(>)}\!=\!D_0^{<(>)}G^{<(>)}$, where $D_0^{<(>)}$ is proportional to the Green's function of the unperturbed phonon bath [19]. More precisely, the mode-space lesser-than self-energy for acoustic phonons and for the nth mode reads [20]

$$\Sigma^{<n,n}_{\mathrm{MS,ac}}(x_i,x_i;E)=\frac{D_{\mathrm{ac}}^2 k_B T}{\rho v_s^2}\sum_m I^{m,n}(x_i,x_i)G^{<m,m}_{\mathrm{MS}}(x_i,x_i;E), \tag{1}$$

where $I^{m,n}(x_i,x_j)=\int dy\int dz|\chi_m|^2(x_i,y,z)|\chi_n|^2(x_j,y,z)$ is the usual form factor, ρ is the material density, v_s is the sound velocity, T is the temperature and D_{ac} is the acoustic deformation potential. Similarly, the lesser-than self-energy for dispersionless optical phonons is expressed as [20]

$$\Sigma^{<n,n}_{\mathrm{MS,opt}}(x_i,x_i;E)=\frac{\hbar D_{\mathrm{opt}}^2}{2\rho\omega_j}\sum_m I^{m,n}(x_i,x_i)G^{<m,m}_{\mathrm{MS}}(x_i,x_i;E\pm\hbar\omega_j)\left[N_j+\frac{1}{2}\pm\frac{1}{2}\right], \tag{2}$$

where ω_j is the frequency of the jth optical branch, D_{opt} is the optical deformation potential and N_j is the equilibrium phonon density given by the Bose statistics. Acoustic and optical phonon parameters for sSi MOSFETs were taken from [21].

Polar optical phonon (POP) scattering was accounted for as a local self-energy similar to Eq. (2) with effective deformation potential D_{pop} and frequency ω_{pop} taken from [13]. This approximation was adopted to circumvent the numerical difficulties of implementing non local-self-energies, which would impede the exploitation of the recursive algorithms to compute the relevant Green's functions elements [22].

The strain was included in our simulations of Tunnel-FETs by adding to the $\mathbf{k}\cdot\mathbf{p}$ Hamiltonian the strain interaction matrix [14], with the four deformation potentials a_v, a_c, b, d taken from [23]. As for sSi MOSFETs, the uniaxial strain was described according to the analytical expressions for the conduction band edges and effective masses reported in [24]. The sSi MOSFETs have a 2% tensile strain in the [100], source-drain direction.

For Tunnel-FETs, instead, we considered tensile biaxial stress, because it is the most effective stress configuration to improve the performance of InAs Tunnel-FETs [12,13]. The stress was always considered uniform inside the source region, whereas it is suppressed at the junction between source and channel according to a gaussian profile:

$$T_{yy}(x)=T_{zz}(x)=Te^{-[(x-x_0)^2/2\sigma^2]}\quad \text{for } x\geqslant x_0, \tag{3}$$

where $T>0$ is the stress magnitude, σ is the standard deviation of the gaussian decay towards the channel region and x_0 is aligned to the source side edge of the gate electrode (see Fig. 2). Throughout the work the stress magnitude for Tunnel-FETs is set to $T=2$ GPa.

4. Simulation results and discussion

We considered rectangular nanowire transistors as sketched in Fig. 1 with the parameters listed in Table 1.

The impact of a uniform strain configuration on the transfer characteristics of InAs Tunnel-FETs was studied in [12,13] and consists in inducing a significant increase of the on current with respect to the unstrained case, but also to induce a current slope degradation in the sub-threshold regime due to the reduced gap and imaginary wave-vector.

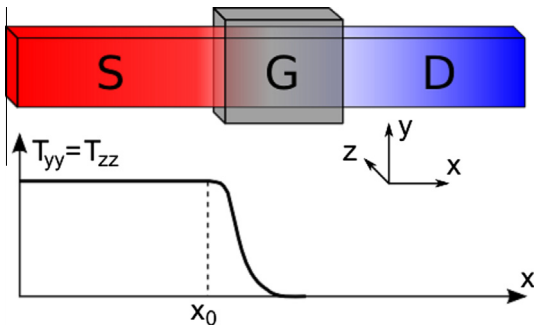

Fig. 2. Sketch of the stress amplitude profile along the longitudinal direction (x axis). The stress amplitude is suppressed starting from the point x_0 according to a Gaussian profile (see Eq. (3)).