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Realizing high voltage SJ-LDMOS with non-uniform N-buried layer

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Abstract

A novel super junction LDMOS (SJ-LDMOS) structure, which reduces substrate-assisted depletion effect, is proposed. The proposed device uses a non-uniform N-buried layer implemented between the SJ region and P substrate to achieve a uniform distribution of surface electric field. Numerical simulation results indicate that the proposed device features high breakdown voltage, low on-resistance. In addition, the proposed device is compatible with smart power technology.

Keywords: LDMOS; Super junction (SJ); Breakdown voltage

1. Introduction

Lateral double-diffused MOSFETs (LDMOST) based on the super junction (SJ) concept were recently proposed to further improve the trade-off characteristics between the breakdown voltage (BV) and the on-resistance (R_{on}) which has always been a major issue in the design of power device [1–6]. The SJ concept is based on achieving charge compensation in the off-state, in a set of alternating and heavily doped n and p pillars comprising the drift region of the device. Provided that the pillars of SJ are fairly narrow and net dopants in both pillars are approximately equal, it is possible to deplete the pillars at relatively low voltage. Upon depletion, the pillars appear to be an "intrinsic" layer and a near uniform electric field is achieved, resulting in a high BV [7–9]. However, the SJ-LDMOS implemented on a substrate suffers from the substrate-assisted depletion effect which degrade the BV of the device.

To eliminate the substrate-assisted depletion effect, in the case of SOI substrate, the unbalanced super junction (USJ) LDMOS on SOI substrate was proposed in which the charge in the n and p pillars are unbalanced such that at the drain end there is a significant excess of charge in the n pillars compared to the p pillars [1]. However, it requires both tight layout and process tolerances. To overcome this, it is possible to use silicon on sapphire (SOS) technology as a dielectric substrate. In that case, the interaction between the substrate and the SJ pillars is eliminated completely [2,3]. Unfortunately, the use of a sapphire substrate is expensive and not mainstream silicon technology. Furthermore, in case of SJ concept on bulk silicon, a SJ-LDMOS with N-buffer layer was developed [4], while this method cannot realize the high breakdown voltage (>600 V). Although, SJ/RESURF LDMOS structure realized the high breakdown voltage [5], it is difficult to form the different doping concentrations for SJ region and RESURF region at one time which significantly increases the cost.

In this paper, a method of suppressing the substrate-assisted depletion effect in SJ-LDMOS implemented on bulk silicon using non-uniform N-buried layer is proposed and analyzed. The BV of proposed SJ-LDMOS can be

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easily achieved more than 600 V even more than 1000 V. Furthermore, the proposed device is compatible with smart power technology without any additional process.

2. Device structure and operation concept

In the conventional SJ-LDMOS, PN junctions are formed between the n-pillars and the P substrate resulting in a vertical electric field component $E_y(x)$ which is a function of lateral position in the drift region. The vertical electric field component gives rise to a surplus of p type charge in the p pillars and upsets the delicate charge balance between the n and p pillars in the off-state [5]. In the proposed SJ-LDMOS (called proposed device) as illustrated in Fig. 1a, a non-uniform N-buried layer is implemented between the SJ region and P substrate in order to suppress the substrate-assisted depletion effect resulting in improving in BV. This is due to the fact that the depletion between the p pillars and the N-buried layer causes the reduction of the charge density in the p pillars which compensates the lack of charge in the n pillars caused by the depletion between the n pillars and p substrate. However, the substrate assisted-depletion effect is most significant near the drain and less effective near the channel. So, the net dose needed of N-buried layer is different between the channel region and drain region. Concretely, there must be a low dose under the channel region but a high dose under the drain region.

The non-uniform N-buried layer can be achieved by using the lateral variation doping technique [10]. This technique uses a layer of oxide or photoresist with a sequence of slit or opening for masking of the impurity implantation. These slits are linearly increased from the channel region toward the drain region. Our group has successfully implemented this technique on double RESURF LDMOS with non-uniform drift region and its BV attains more than 700 V [11,12]. The proposed device is compatible with smart power technology. The non-uniform N-buried layer is realized by masked implantation of phosphorus in the P substrate as shown in Fig. 1b before the epitaxial layer is formed on substrate. The annealing process after this ion-implanted can be realized simultaneously with the following high temperature processes such as field oxide formation. It is not necessary for the longer diffusion time and higher diffusion temperature to form the dopants implanted punch-through between the adjacent masking openings. Then the alternate n and p pillars of SJ drift region and other processes are formed like these of conventional SJ LDMOS.

3. Results and discussion

To demonstrate the performance advantages of the proposed SJ-LDMOS devices, 3D simulations were carried out using DESSIS-ISE [13]. In addition, in order to highlight the key points of the proposed device, we also simulated a conventional SJ-LDMOS device (called conventional device) under the same conditions. The difference between them is only to implement the non-uniform N-buried layer or not. We will compare the performance at the following device parameter ($L_d = 40$ μm, $N_D = N_A = 2 \times 10^{16}$ cm^{-3}, $W_n = W_p = 1$ μm, $T_e = 5$ μm, $N_{SUB} = 1 \times 10^{13}$ cm^{-3}) and the non-uniform N-buried layer dose for the proposed device is 2.0×10^{12} cm^{-2}.

Fig. 2a and b shows the potential distributions at the BV for the conventional device and the proposed device, respectively. It is clear that the space of the equipotential lines in the proposed device is more uniform than that of its counterpart, which results in a breakdown voltage of 667 V in proposed device compared with that of 228 V in conventional SJ-LDMOS. For the conventional one, the doping concentrations of n (N_D) and p (N_A) pillars are both 2×10^{16} cm^{-3}, which satisfy the RESURF condition. However, because of the substrate-assisted depletion effect, the depletion is not enough and the high electric field occurs near the drain end as shown in Fig. 3. On the other hand, for the proposed one, a non-uniform N-buried layer is implemented, which provides the additional charge for compensating the charge imbalance in n pillars due to the substrate-assisted depletion effect. This means that a fairly uniform electric field is achieved at breakdown voltage for the proposed device as shown in Fig. 3.

The dose Q_B of the N-buried layer is important parameter in the design of the proposed device. Fig. 4 shows the dependences of the BV on the dose Q_B of N-buried layer. It is clearly shown that there is an optimal value Q_B for the

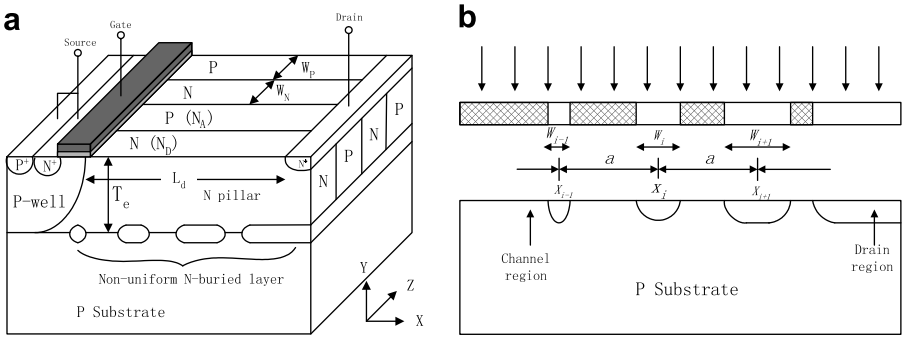

Fig. 1. (a) Three-dimensional view of the proposed device and (b) schematic of the mask used to obtain the non-uniform N-buried layer.