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Formation, etching and electrical characterization of a thermally grown gallium oxide on the Ga-face of a bulk GaN substrate

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Abstract

Thermal oxides on the Ga-face of low defect density bulk gallium nitride (GaN) were controllably produced under varying conditions and subsequently analyzed. The thermal oxidation was performed in a dry oxygen atmosphere at different temperatures and different oxidation times. Each oxide layer was identified as the monoclinic β-Ga_2O_3 by a θ–2θ X-ray diffraction (XRD) scan. Complementary Auger electron spectroscopy (AES) and high-resolution X-ray photoelectron spectroscopy (XPS) were also performed to study the chemical and electronic states of the oxide. The surfaces of the as-grown oxide and the GaN surfaces (after oxide removal) were studied using scanning electron microscopy (SEM). The roughness of both surfaces was found to increase with increasing oxidation temperature. Schottky diodes were fabricated on the GaN surfaces after oxide removal to further examine the surface quality. An excess reverse leakage current was found for Schottky diodes fabricated on GaN surfaces that were oxidized at 950 °C or 1000 °C, indicating possible surface decomposition at these two temperatures. The characteristics of wet and dry etching of the gallium oxide layer were also investigated. Finally, metal–oxide–semiconductor (MOS) capacitors were fabricated using thermally oxidized bulk GaN substrates. Current–voltage (*I*–*V*) measurements showed a low reverse current of 1.5 pA at −10 V. The oxide breakdown field was determined to be 0.65 MV/cm. Capacitance–voltage (*C*–*V*) measurements displayed a deep depletion feature, and the interface trap density near the conduction band was estimated to be in the low 10^{11} eV^{-1} cm^{-2} range.
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Keywords: GaN; Free-standing substrate; Thermal oxidation; Wet chemical etching; Reactive ion etching; MOS; Interface trap density

1. Introduction

GaN has received much attention recently in the area of optoelectronics, especially for the fabrication of high-efficiency blue/green and ultraviolet (UV) light-emitting diodes (LEDs). Its fundamental physical properties, such as a large band gap (3.4 eV), high breakdown field (4 MV/cm) and high electron saturation velocity (3×10^7 cm/s), also make GaN a promising material for high power, high temperature applications. GaN metal–semiconductor field effect transistors (MESFETs) and GaN/AlGaN heterostructure field effect transistors (HFETs) with promising device characteristics have been fabricated, and their potential for high power, high temperature application has been demonstrated [1–3]. However, one of the major factors that limit

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the performance and reliability of these devices for high power applications is their relatively high gate leakage, which for Schottky contacts is worse at high temperatures. To avoid this problem, significant progress has been made for the metal–oxide–semiconductor (MOS) or metal–insulator–semiconductor (MIS) structures. The use of an insulated gate is expected to reduce gate leakage and power consumption in the gate circuit. Ren et al. [4] reported fabrication procedures and electrical characteristics for the first GaN-based metal–oxide–semiconductor field effect transistor (MOSFET) using a gate dielectric comprised of deposited $Ga_2O_3(Gd_2O_3)$. Since then, several approaches have been employed to develop GaN-based MOS or MIS system using deposited insulators such as SiO_2 [5], Si_3N_4 [6], MgO [7], Sc_2O_3 [8], Ta_2O_5 [9] and Al_2O_3 [10]. One of the drawbacks of these deposited oxides for MOSFET applications is the relatively high interface trap density at the insulator/GaN interface, typically the order of mid $10^{11}\ eV^{-1}\ cm^{-2}$–$10^{12}\ eV^{-1}\ cm^{-2}$. Thermal oxidation has been the most useful method for oxide growth as a gate dielectric in Si-based MOS technology due to advantages such as low interface trap density and fabrication simplicity. Despite a higher interface trap density compared to SiO_2/Si, thermal oxidation is also the preferred method for SiC-based MOS technology. However, for some compound semiconductors, thermal oxidation is much more complicated. For example, the growth of high quality thermal oxides for GaAs is hindered by the competing formation of Ga_2O_3 and As_2O_3 as well as by the presence of excess elemental As at the oxide/GaAs interface, which results in a poor interfacial properties [11]. Fortunately, for GaN, nitrogen and its oxides are volatile, and only gallium oxide remains after oxidation. However, care must be taken as for the oxidation temperature. No (or minimal) oxide growth is observed for temperatures below 750 °C [12]. On the other hand, GaN is thermally unstable at temperatures above 1000 °C [13]. Recently, there have been a few initial reports of GaN MOS structures based on thermally oxidized GaN epitaxial layers on sapphire substrates [14,15]. The thermally grown β-Ga_2O_3/GaN interface indeed displayed a lower interface trap density by more than one order of magnitude compared to other deposited insulator/GaN interfaces. This looks promising for GaN MOSFET fabrication.

Recent development in hydride vapor phase epitaxy (HVPE) technology has enabled the growth of free-standing GaN wafers with a very low dislocation density ($<5\times10^6\ cm^{-2}$). Thermal oxidation has, until now, not been reported on bulk GaN substrates. In this paper, we report the results of a comprehensive investigation of the oxidation kinematics, material characterization, surface analysis, wet or dry etching and electrical characterization of thermally grown Ga_2O_3 on bulk GaN.

2. Experimental

The free-standing GaN substrates used in this study were synthesized by a hydride vapor phase epitaxy (HVPE) process. The substrates are 10 mm × 10 mm square and 265 μm thick. *C–V* measurements showed an unintentional *n*-doping level of $\sim5.5\times10^{16}\ cm^{-3}$. The Ga-terminated surface (front side) was polished with a typical dislocation density of $5\times10^6\ cm^{-2}$. Prior to oxidation, the samples were ultrasonically cleaned sequentially in trichloroethylene (TCE), acetone, and methanol for 5 min each, then dipped into a heated HCl: H_2O (1:1) (∼100 °C) for 10 min, and finally rinsed in de-ionized water and blown dry using N_2. Before the samples were loaded into a horizontal quartz tube furnace, the furnace temperature was stabilized at 300° below the chosen oxidation temperature, and the system was purged with dry O_2 for 15 min. Then, the samples were placed in a quartz boat and transferred to the center of the quartz tube and kept there for 15–20 min to allow the temperature of the sample to equilibrate with the ambient. The furnace temperature was then increased to the oxidation temperature at a rate of 5 °C/min. Oxidations were performed at 850 °C, 900 °C, 950 °C and 1000 °C with varying oxidation times (4–12 h). Since the oxidation rate is negligible when the temperature of the sample is below 750 °C, the ramping time was not counted in the time of oxidation. The O_2 gas flow rate was maintained at 500 sccm for the entire process. After oxidation, the samples were removed from the furnace tube and cooled to room temperature in air.

The structural and chemical properties of the oxidized samples were analyzed by X-ray diffraction (XRD), Auger electron spectroscopy (AES), X-ray photoelectron spectroscopy (XPS) and scanning electron microscopy (SEM) measurements. Wet chemical etching was explored using an HCl-based solution at different temperatures. For reactive ion etching (RIE), NF_3 or Cl_2/Ar based discharges were used. The fabrication processes of the MOS capacitors can be briefly described as follows. First, the oxide grown on the backside of the substrate was removed by RIE. Then, a full backside ohmic contact of Ti (50 nm)/Al (100 nm) was deposited by sputtering, followed by rapid thermal annealing at 850 °C for 1 min in a nitrogen atmosphere. Finally, 210 μm diameter Mo contacts (100 nm thick) were sputtered onto the oxide surface as gate electrodes. Current–voltage measurements were performed using a Keithley picoammeter and *C–V* measurements were performed at 1 MHz using a Keithley simultaneous hi-lo *C–V* system.

3. Results and discussion

Fig. 1 shows the X-ray diffraction pattern (θ–2θ scan) for an oxide which was grown on bulk GaN at 900 °C for 10 h. In addition to the characteristic diffraction peaks for GaN (002) and (004), additional peaks that are associated with the thermal oxide were observed. Comparing with the *powder diffraction file*, 11-370., the strongest two peaks were identified as the peaks due to the reflection from the (−113) and (−306) planes of monoclinic β-Ga_2O_3. Similar diffraction patterns were also observed from sam-

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