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AlGaN/GaN metal oxide semiconductor high electron mobility transistor using liquid-phase deposited strontium titanate

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ABSTRACT

$SrTiO_3$ thin films were deposited on AlGaN/GaN wafer by a simple, low-temperature liquid-phase deposition (LPD) method, and applied as the gate dielectric in metal oxide semiconductor high electron mobility transistor (MOSHEMT). X-ray diffraction and electrical characteristics were measured to investigate the film phase and leakage current. AlGaN/GaN MOSHEMTs with 20 nm-thick $SrTiO_3$ as the gate dielectric were also fabricated. Compared with its counterpart HEMT, MOSHEMT shows lower leakage current and larger breakdown voltage. The suppressed gate leakage current improves both I_{on}/I_{off} ratio and subthreshold slope. Larger maximum drain current density could be achieved with higher V_{on} in the MOSHEMT. Flatter transconductance and wider gate voltage swing of the MOSHEMT demonstrate better device linearity. The lower low-frequency noise is obtained due to the lower surface states.

1. Introduction

GaN-based HEMTs have attracted much attention for application in high-frequency and high-power devices due to the large bandgap, high saturated electron velocity, and high breakdown electric field. However, Schottky gate in HEMT usually results in higher gate leakage. The leakage can be avoided by incorporating thin insulator films into the interface between the gate metal and the semiconductor [1,2]. The inserted thin films also result in the decrease of transconductance and the shift of threshold voltage due to the decreased gate-to-source capacitance with the increased gate-to-channel distance. These problems can be overcome by maintaining a high gate-to-source capacitance, which can be achieved by using a high-k material as a gate dielectric. In recent years, several high-k materials such as Al_2O_3, La_2O_3, HfO_2, and ZrO_2 [3–7] have been investigated as gate dielectrics in GaN-based MOSHEMT and showed the better characteristics than conventional SiO_2. Therefore, a higher-k material than these conventional high-k materials may further improve MOSHEMTs in the further scaled devices. Compared with the other materials, $SrTiO_3$ shows great potential as a gate dielectric for its thermal stability [8] and high dielectric constant which can be higher than 100 according to crystalline phase. It has been demonstrated that $SrTiO_3$ serves as a gate dielectric for Si-based devices [9,10]. However, there is still very limited research about $SrTiO_3$ on AlGaN/GaN HEMT [11] and no device characteristics were shown.

Several methods for depositing $SrTiO_3$ oxide films have been presented, including plasma-enhanced ALD [12], MBE [13], sputtering [14], and electron beam evaporation [15]. However, all these methods are based on a vacuum system and composed of multistep processes. The method used in this work, referred to as liquid-phase deposition (LPD), provides a low-cost, low-temperature, and simple method to form oxide layers [16]. It utilizes ammonium hexafluorotitanate $(NH_4)_2TiF_6$ and H_3BO_3, with an $Sr(NO_3)_2$ aqueous solution serving as source liquid. In the method, the relatively low deposition temperature effectively avoids thermal strain and defects [17,18], and the deposition rate can be controlled to achieve nanometer scalability. Several kinds of thin films such as TiO_2, Ba-doped TiO_2, and Al_2O_3 deposited by LPD have been investigated on GaN-based devices, and have shown good characteristics of leakage current and interface trap density [19–22]. In this study, we introduced the deposition of $SrTiO_3$ on GaN as the gate dielectric and probed the performance of the fabricated $SrTiO_3$/AlGaN/GaN MOSHEMT.

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2. Experimental

Through the LPD method, $SrTiO_3$ thin films of 70 nm thickness were deposited at a temperature of 40 °C on the n-type GaN with a doping concentration of 3×10^{17} cm^{-3} for physical and chemical analyses. The deposition rate is about 1.2 nm/min. The LPD solution was prepared as follows. A 0.2 M concentration of $(NH_4)_2TiF_6$ solution was first prepared by adding $(NH_4)_2TiF_6$ powder into 25 mL deionized water and stirring it for 10 min. Next, 25 mL 0.6 M H_3BO_3 solution and 5 mL 0.2 M $Sr(NO_3)_2$ solution were mixed into the $(NH_4)_2TiF_6$ solution and stirred for 10 min. The device sample was then floated in the solution with the surface upside down. This prevented particles formed in the solution from accumulating on the sample surface. In the previous study, the X-ray photoelectron spectroscopy (XPS) measurement has showed that the films corresponding to $SrTiO_3$ [23]. While $SrTiO_3$ thin films are applied as gate dielectric, it is important to deposit amorphous films to suppress the grain boundaries-induced leakage paths [24]. Therefore, X-ray diffraction (XRD) and electrical characteristics were measured on as-deposited $SrTiO_3$ films annealed at 400 °C and 600 °C to investigate phase transformation and leakage current. The MOS structure of $SrTiO_3$/n-type GaN was fabricated to study the leakage current. The contact electrode of Ni/Au was deposited on the $SrTiO_3$ films to form the MOS structure with an area of 1×10^{-4} cm^2.

Fig. 1 shows the schematic cross-sectional view of the fabricated $SrTiO_3$/AlGaN/GaN MOSHEMT on Si substrate prepared by metal organic chemical vapor deposition (MOCVD). A 0.8 μm thick undoped GaN layer was grown on the 1.4 μm thick GaN buffer layer, followed by a 20 nm thick undoped $Al_{0.26}Ga_{0.74}N$ layer and a 2.5 nm thick undoped GaN capping layer. The measured sheet concentration was 1.06×10^{13} cm^{-2} with the mobility of 1373 cm^2/V s from Hall measurement. For device fabrication, device isolation was accomplished by inductively-coupled plasma reactive ion etching (ICP-RIE) using Cl_2 and BCl_3 gas. Source/drain region was patterned by conventional optical lithography, and ohmic contact metal of Ti/Al/Ni/Au was deposited and annealed in N_2 atmosphere. The measured contact resistivity was 0.3 Ω mm from transmission line method (TLM). Then, $SrTiO_3$ thin films of 20 nm were deposited on the sample by LPD. Finally, the gate metal of Ni/Au was deposited. The devices were fabricated with gate width/length (W/L) of 100 μm/0.5 μm. Gate-to-drain distances and gate-to-source distances were both 1 μm. I–V and C–V characteristics of the device were measured by B1500A and HP4280, respectively.

3. Results and discussions

XRD measurement shown in Fig. 2 indicates that there are no other peaks except the as-deposited $SrTiO_3$ films peak on the GaN. The amorphous $SrTiO_3$ films are still stable even if the annealing temperature is increased to 400 °C for 20 min. Two peaks of $SrTiO_3$ films are observed after annealing at 600 °C for 20 min, which correspond to the rutile and tetragonal anatase phase (200) [16]. For the MOS structure, the leakage current characteristics are shown in Fig. 3. The film thickness of as-deposited $SrTiO_3$ was 70 nm, which decreased to 52 nm after annealing at 400 °C and to 44 nm after annealing at 600 °C. The obvious decrease of film thickness is due to the less dense films from LPD system. After annealing at 400 °C, the leakage current density is significantly better and about 4.2×10^{-9} A/cm^2 at −1 MV/cm and breakdown voltage is more than −4 MV/cm. However, the leakage current density increases to 1.1×10^{-3} A/cm^2 at −1 MV/cm after annealing at 600 °C. The large leakage current is due to the LPD-$SrTiO_3$ films changing from the amorphous to the anatase and rutile phases after annealing at 600 °C creating the leakage path at the grain boundaries [24].

Fig. 4 shows the cross-sectional transmission electron microscope image of as-deposited $SrTiO_3$ on the AlGaN/GaN device structure. The smooth interface without dislocations between $SrTiO_3$ and device structure is also observed.

To investigate the surface roughness of oxide films, atomic force microscopy (AFM) was used to analyze $SrTiO_3$ films before and after annealing. The 3D images of 1 μm × 1 μm area are shown in Fig. 5. The RMS values were improved from 2.7 to 1.5 nm for $SrTiO_3$ films annealed at 400 °C, respectively. Quite large surface roughness improvement can be obtained after annealing due to the less dense films. However, with increasing annealing temperature of 600 °C, the increased grain size and crystal phase transformation lead to the rougher surface of 2.4 nm [25].

Fig. 6a shows three terminal off-state breakdown characteristics and leakage current of the conventional HEMT and MOSHEMT with a gate dielectric of 20 nm. Compared with the HEMT, the leakage current can be reduced by more than two orders of magnitude in the MOSHEMT, which is comparable to the Al_2O_3 MOSHEMT [26]. The film thickness of high-k $SrTiO_3$ can be increased to suppress the leakage current while maintaining the high capacitance. In Fig. 6b, the gate leakage current remains low in the order of 1.29×10^{-6} mA/mm even at a gate bias of −100 V in the MOSHEMT. By contrast, a significant increase of gate leakage current is observed in the HEMT while V_{GD} is close to −100 V. The V_{on} increases from 0.6 V to 1.3 V in

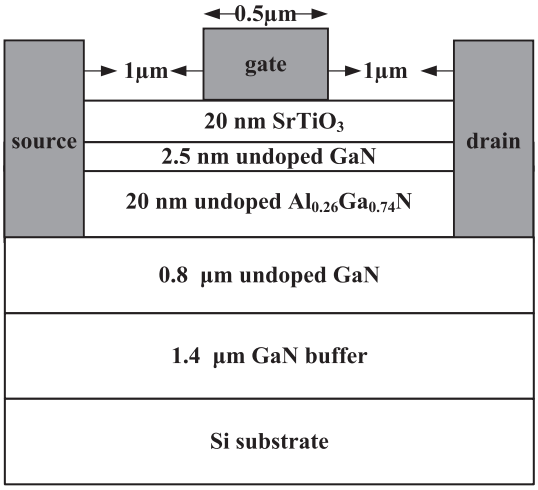

Fig. 1. The device schematic cross-section view of the $SrTiO_3$/AlGaN/GaN MOSHEMT.

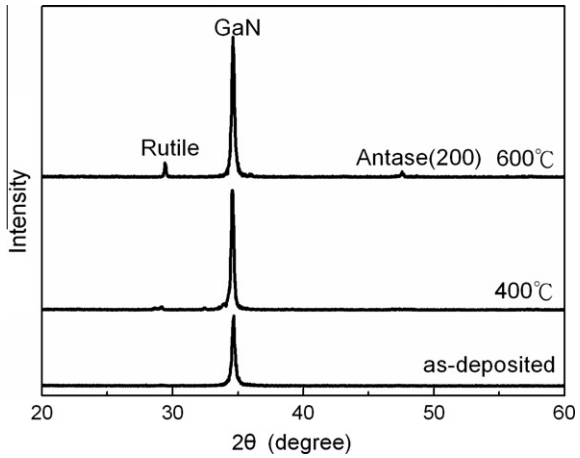

Fig. 2. The XRD analysis of as-deposited $SrTiO_3$ films and $SrTiO_3$ films annealed at 400 and 600 °C for 20 min.