



Characterization of residual implant damage by generation time technique

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ABSTRACT

The quality of an implanted layer was characterized using non-contact generation lifetime. This technique does not require fabrication of any junction devices or MOS capacitors. The generation lifetime is measured by monitoring the surface voltage decay during collapsing of the deep depletion created by a pulse of corona charge placed on the wafer surface. The voltage decay, measured with the vibrating Kelvin probe, is due to the generation of minority carriers similar to the capacitance transient measurement of generation lifetime in MOS capacitors. Residual implant damage is manifested by faster generation rate and therefore faster voltage decay rate. Generation lifetime is measured versus implant energy and annealing temperature.

The corona based generation lifetime technique yields additional useful parameter namely dopant concentration. The dopant concentration is calculated from the breakdown voltage and is determined by the implant distribution and depletion width at breakdown conditions.

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1. Introduction

When silicon wafers are processed at high temperatures, thermally induced stress can create defects that deteriorate electrical device properties. These lattice defects are frequently followed by crystal dislocation and slip, thus resulting in further degradation of the Si electrical quality.

In CMOS processing, a relationship has been reported between the device performance, such as refresh time, and the silicon defects induced by the shallow trench isolation (STI) process [1,2]. In addition to STI, it is also important to control contact etch and implantation processes to suppress the electrical degradation. Furthermore, as CMOS devices continue to aggressively shrink, control of such non-visual defects, especially those existing in the near surface region of silicon, become even more important.

Silicon lattice defects can be monitored directly in the Silicon using optical microscopy, TEM, and XRT, or alternatively through electrical characterization of IC devices using specifically prepared testing modules. However, these methods are not readily extend-

able for in-line detection of non-visual defects that are smaller than slip and dislocations.

On the other hand, generation lifetime, τ_g , is an electrical material parameter that is suitable to characterize the quality of silicon surface layer. It has been applied to characterize epitaxial films [3]. A common method to measure generation lifetime is the pulsed MOS capacitor technique [4,5]. Recently, a non-contact adaptation of the technique was proposed [6,7]. A more detailed review of generation lifetime measurement technique can be found in [8]. The doping concentration must be known to obtain generation lifetime from the non-contact corona – Kelvin approach. Doping concentration can be obtained from another measurement. For example $Q^2 - V$ or ac-SPV measurements can be used to measure doping concentration in a non-contact fashion. We propose to measure doping concentration from the value of avalanche breakdown voltage in semiconductor. This greatly simplifies measurement apparatus and allows us to obtain generation lifetime and doping concentration from a single voltage decay.

In this paper we discuss the corona based generation lifetime technique and apply it to quantify residual implant damage after a deep n -well implant step. The non-contact nature of the corona-based generation lifetime technique makes it suitable for in-line implementation.

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2. Experimental

2.1. Sample preparation

Phosphorous implantation into a *p*-type bare Si substrate was carried at a fixed dose of 2×10^{13} ions/cm². Two implant energies, 0.8 and 1.2 MeV, were used to control the depth of a *n*-well. Three sample sets composed of two wafers each were prepared. Implant activation was carried out in a RTA chamber, and three different thermal processes were used. During RTA annealing, implant was activated and some of the defects were annealed. Following implant anneal, sample oxidation was carried out to grow ~ 10 nm oxide layer. A *n*-type CZ silicon wafer was also oxidized to provide reference, damage-free surface. Sample conditions are summarized in Table 1.

2.2. Measurement apparatus

The apparatus shown schematically in Fig. 1 consists of (1) a corona gun, which is used to deposit corona charge on the wafer surface; (2) Kelvin probe, which is used to measure the voltage transient after charging; and (3) a stage, which moves the measured site on the wafer between the corona gun and the Kelvin probe. The apparatus is essentially the same as that used for non-contact corona Kelvin based metrology and is discussed in Refs. [8–10]. When taking data, the entire apparatus is enclosed in a dark chamber to prevent photogeneration of carriers.

Two factors are important for selection of corona dose: (1) charge leakage across the dielectric layer, and (2) avalanche breakdown in silicon [11]. For the purpose of generation lifetime measurements, charge leakage across the dielectric layer is a parasitic effect which has to be minimized or accounted for [12]. It will cause oxide voltage change versus time, thus affecting extraction of the decay rate in silicon (see Eq. (2) below). For a 10 nm oxide layer, charge leakage is determined by the Fowler–Nordheim tunneling current. To avoid corona charge neutralization due to the Fowler Nordheim current, electric field across the oxide should not exceed ~ 5.5 MV/cm [13]. This defines the upper limit for corona charge at $\sim 1.2 \times 10^{13}$ charges/cm² (or 1.9×10^{-6} C/cm²).

Table 1
Sample conditions of deep *n*-well and *n*-type bare Si wafers.

Substrate	Implant dose	Implant energy	RTA	Oxide
<i>p</i> -Type	2×10^{13} ions/cm ²	1.2 MeV	1000 °C 10 s + 1000 °C 30 min	10 nm
		0.8 MeV		
		1.2 MeV	1000 °C 10 s + 950 °C 30 min	
		0.8 MeV		
		1.2 MeV	1000 °C 10 s	
<i>n</i> -Type	None	None	None	

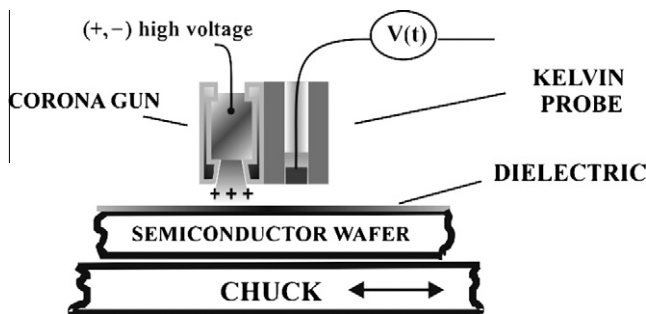


Fig. 1. Schematic of corona – Kelvin apparatus for generation time measurements.

To achieve avalanche breakdown corona charge should be equal to or greater than the depletion space charge, Q_{SC} , at the avalanche voltage. In general, Q_{SC} increases with increasing doping level. For example, for doping concentrations 1×10^{15} cm⁻³ and 1×10^{17} cm⁻³, the depletion space charge is 2.6×10^{12} charges/cm² and 3.9×10^{12} charges/cm² respectively. It can be seen that the depletion space charge has only a weak dependence on the doping concentration. It should be noted that when $Q_C > Q_{SC}$, the corona charge in excess of the depletion space charge at breakdown is quickly neutralized by the avalanche breakdown current.

The above boundary conditions constrain the corona dose to a practical range of $\sim 4 \times 10^{12}$ charges/cm² to $\sim 1.2 \times 10^{13}$ charges/cm². The corona charge $\sim 7 \times 10^{12}$ charges/cm² (corresponds to 1.1×10^{-6} C/cm²) was used in our study. It is large enough to achieve the avalanche breakdown condition in silicon and low enough not to cause excessive charge leakage across dielectric.

3. Theory and calculation

3.1. Generation lifetime

Generation lifetime is measured by monitoring the surface voltage decay during collapsing of the deep depletion created by a pulse of corona charge placed on the wafer surface. The measured voltage is referred to as the contact potential difference, V_{CPD} . It is equal to the probe-semiconductor work-function difference that includes the *n*-*p* junction built-in voltage, the voltage drop across the surface depletion barrier, V_{SB} , and the voltage drop across the top surface dielectric, V_{OX} :

$$V_{CPD} = V_{SB} + V_{OX} + \phi_{ms} \quad (1)$$

The silicon is biased into deep depletion conditions by a pulse of corona charge of appropriate polarity. Positive corona charge is used to bias *p*-type silicon, while negative charge is used to bias *n*-type silicon. An example of the contact potential voltage decay versus time is shown in Fig. 2. After deposition of corona charge, V_{CPD} is equal to:

$$V_{CPD} = (V_{SB} + \Delta V_{SB}) + (V_{OX} + \Delta V_{OX}) + \phi_{ms} \quad (2)$$

The deep depletion that is generated is a non-equilibrium condition for the semiconductor, however it will relax to the equilibrium condition due to the thermal generation of electron-hole pairs. The decay from deep depletion is accompanied by a build up of a surface inversion layer. This is necessary to satisfy charge neutrality between corona charge and the charge in the

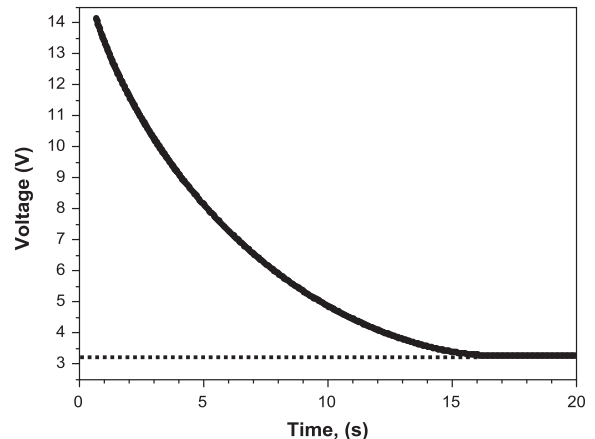


Fig. 2. Example of voltage decay from the deep depletion condition.

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