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Scaling challenge of Self-Aligned STI cell (SA-STI cell) for NAND flash memories

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ABSTRACT

This paper describes scaling limitations and challenges of Self-Aligned STI cell (SA-STI cell) over 2X–0X nm generations for NAND flash memories. The scaling challenges are categorized to (1) narrow Read Window Margin (RWM) problem, (2) structural challenge, and (3) high field (5–10 MV/cm) problem. First, (1) the narrow RWM is investigated by extrapolating physical phenomena of FG–FG coupling interference, Electron Injection Spread (EIS), Back Pattern Dependence (BPD), and Random Telegraph Noise (RTN). The RWM is degraded not only by increasing programmed Vt distribution width, but also by increasing Vt of erase state mainly due to large FG–FG coupling interference. However, RWM is still positive in 1Z nm (10 nm) generation with 60% reduction of FG–FG coupling by air-gap process. For (2) structural challenge, the Control Gate (CG) fabrication margin between Floating Gates (FGs) is becoming much severer beyond 1X nm generation. Very narrow 5 nm FG width/space has to be controlled. For (3) high field problem, high field between CGs (word lines; WLs) is critical during program. By using WL air-gap, high field problem can be mitigated, and 1Y/1Z nm generation seems to be realized. Therefore, the SA-STI cell is expected to be able to scale down to 1Z nm (10 nm) generation, with the air gap of 60% reduced FG–FG coupling interference and an accurate control of FG/CG formation process.

1. Introduction

The production volume of NAND flash memory [1] is tremendously increasing with extensive applications, such as smart phone, tablet PC, and Solid-State Drive (SSD). The market size is expected to be over $25 Billion in 2012. In order to satisfy requirements of these applications, low cost and high reliable NAND flash memory has been intensively developed over 25 years. The scaling trend of NAND flash memory cell is shown in Fig. 1. LOCOS isolation was used for 0.7–0.3 μm generation [2]. However, LOCOS isolation had a critical limitation of isolation width of around 0.8 μm due to applied high voltage (~8 V) between active areas [2]. Then Shallow Trench Isolation (STI) was applied to NAND Flash. As a suitable memory cell structure for NAND Flash, the Self-Aligned STI cell (SA-STI cell) had been developed [3–6] and implemented to NAND flash products [7]. This technology can reduce isolation width from 2F @ LOCOS (F; Feature size) to F @ SA-STI, so cell size can be scaled down to ideal $4F^2$ [3]. As the first generation of SA-STI cell, the SA-STI cell with Floating Gate (FG) wing was used to increase coupling ratio and to decrease structure aspect ratio [4,5], as shown "SA-STI w/FG wing" in Fig. 1. After that, from 90 nm generation, the SA-STI cell with a single layer FG had started to use to avoid small tolerance of FG alignment, as the second generation of SA-STI cell [3]. Furthermore, the effective cell size can be reduced by Mu1ti-Level Cell (MLC, TLC, QLC). Therefore, small cell size of $4F^2$ combined with Mu1ti-Level Cell can drastically reduce the bit cost.

The fabrication of the SA-STI cell is simple and uses only conventional techniques, as shown in Fig. 2 [3]. The floating gate and STI patterning are carried out by the same mask, so the number of fabrication steps for the SA-STI process can be decreased with about 10% in comparison with that for a conventional LOCOS process. In addition, this technology has also demonstrated an excellent reliability, because the FG does not overlap the STI corner because FG over the tunnel oxide is patterned as the shape of the active area. The programming and erasing characteristics became much uniform and stable [3–5]. Therefore, the SA-STI cell has very high reliability and high performance [3–7].

The SA-STI cell structure and process have been used more than 10 years and 10 generations. Fig. 3 shows a TEM cross section of recent mid-1X nm SA-STI memory cells [8]. However, for further scaling a SA-STI cell beyond mid-1X-nm generation, it is becoming hard to scale down due to facing the many physical limitations, such as FG–FG coupling interference [9], Random Telegraph Noise (RTN) [10–12], CG formations between FGs [13], and WL high field problem, and reducing number of stored electrons [14].

In this paper, several scaling problems and limitations have been discussed. As a result, the SA-STI cell could be scaling down

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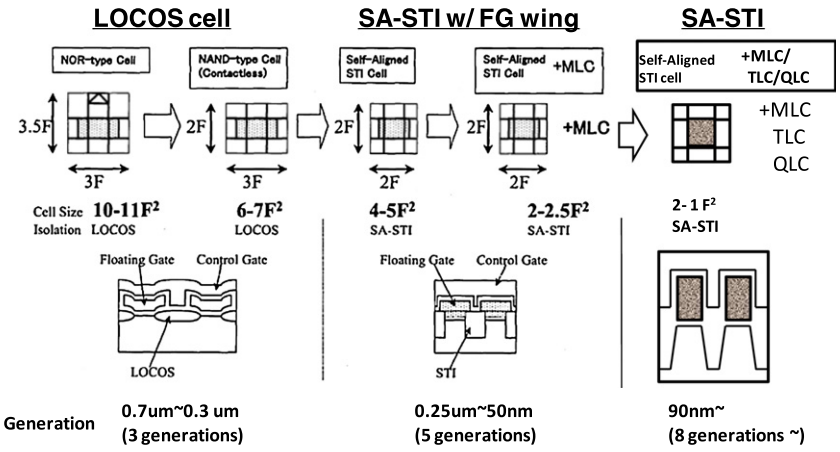

Fig. 1. The scaling trend of NAND flash memory cell. The key technologies to scale down cell size were the Self-Aligned STI cell (SA-STI cell) and multi-level cell (MLC, TLC, QLC) scheme.

to 1Z nm (10 nm) generation with an accurate control of FG/CG formation process and air gap process to manage FG–FG coupling interference and WL high field problem.

2. Scaling challenge of SA-STI cells

2.1. Assumption of dimension scaling

Fig. 4 shows a top view of conventional NAND cell string. In order to investigate the scaling of the SA-STI cell, cell dimensions beyond 2X nm (26 nm) generation are assumed, as shown in Table 1. Dimensions of 2X nm are given, 27 nm for the Bit Line (BL) half pitch and 26 nm for the Word Line (WL) half pitch. Dimensions beyond 2X nm are assumed to scale down by fixed scaling factor of $x0.85$ for BL half pitch and $x0.8$ for the WL half pitch. And also the channel width W and Inter-Poly Dielectric (IPD) thickness are assumed to scale down by the factors of $x0.9$ and $x0.95$, respectively.

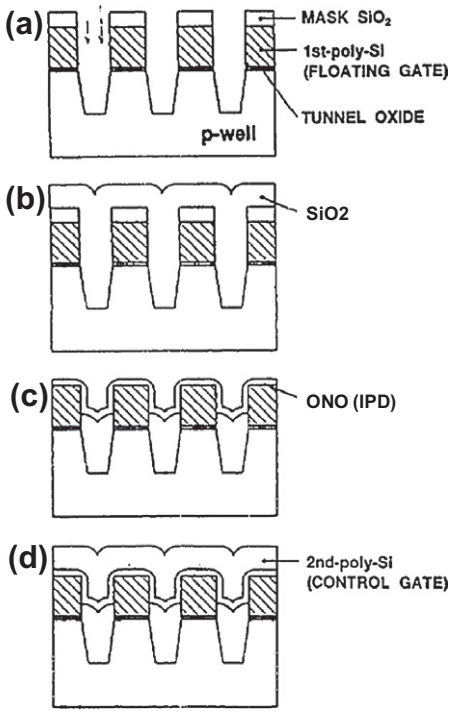

Fig. 2. The process sequence of the SA-STI cell [3]. (a) Floating gate (FG) poly-Si etching and Si Trench etching. (b)SiO2 fill in STI, (c) Oxide etch-back and ONO (IPD) formation, (d) Control Gate (CG) formation. The floating gate and STI patterning are carried out by the same mask, so the Floating gate does not overlap the STI corner. Then SA-STI cell has excellent reliability.

2.2. Assumption for investigating Read Window Margin (RWM)

Fig. 5 shows an image of read Vt window in MLC (2bit/cell) NAND cell. The "Vt window" is defined by a right-side edge of erase distribution and a left-side edge of L3 (highest programmed state) after completing all pages program operation in block (strings). Two programmed Vt distribution of L1/L2 have to be inside of the Vt window to be reliable read operation. Read Window Margin (RWM) is defined by RWM = (Vt window) – 2 * (Programmed Vt distribution width), so that RWM means the separation margin of Vt distributions.

As cell scaling, the RWM had been seriously degraded as scaling down from 0.7 μm to 2X nm generation, because several physical phenomena were getting worse. Therefore, for further scaling of NAND cell, it is very important to analyze and foresee the RWM in future scaled NAND cell. In order to investigate RWM, the scaling trend of physical phenomena of Electron Injection Spread (EIS) [15–17], FG–FG coupling interference [9], RTN [10–12], and Back Pattern Dependence (BPD) are assumed as following. And other assumptions of the page program sequence, parameter setting, etc., are also shown in following.

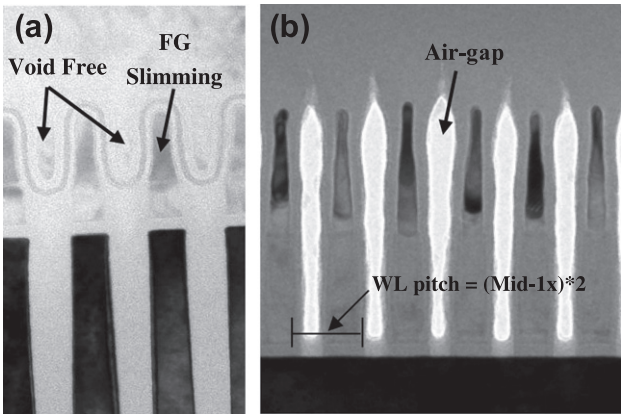

Fig. 3. TEM photograph of mid-1X nm SA-STI NAND flash cells [8].