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Analytical model for ultra-thin body junctionless symmetric double gate MOSFETs in subthreshold regime

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ABSTRACT

In this paper, we propose an approximate solution to solve the two dimensional potential distribution in ultra-thin body junctionless double gate MOSFET (JL DG MOSFET) operating in the subthreshold regime. Basically, we solved the 2D-Poisson equation along the channel, while assuming a parabolic potential across the silicon thickness, which in turn leads to some explicit relationships of the subthreshold current, subthreshold slope (SS) and drain induced barrier lowering (DIBL). This approach has been assessed with Technology Computer Aided Design (TCAD) simulations, confirming that this represents an interesting solution for further implementation in generic JL DG MOSFETs compact models.

1. Introduction

JUNCTIONLESS DOUBLE GATE MOSFET is one of the most promising alternative architecture for CMOS technology due to its immunity to short channel effects (SCEs) and outstanding characteristics [1]. Today, formation of source/channel and drain/channel junctions is one of the most important problems which has been a critical issue in designing short channel devices. This technological issue can be overcome in junctionless transistors (JLTs), which typically consist of a uniformly doped silicon layer (*n* or *p* type) between two gates, just as the double gate MOSFETs, but where the source and the drain have the same doping type as the channel [2]. Therefore, JL FETs need neither lateral abrupt doping, nor high thermal budget, thus making manufacturing simpler.

Reported characteristics exhibit excellent turn-on and output characteristics in JL DG MOSFETs [1,2]. In addition, more recently, also lower drain induced barrier lowering (DIBL) in junctionless DG MOSFET technology [3] has been demonstrated with respect to the junction based devices. However, it has also been reported [4] that the overall subthreshold behavior could be significantly impacted by random dopant fluctuation effect in junctionless devices having high doping levels in the channel (greater than 10^{19} cm^{-3}), but still this effect is expected to be less severe for finer technology generations. Regarding these benefits, it is very likely that these devices will be used in future nanoscale CMOS based technology. For that reason, there is also a need for developing complete compact models for large scale simulations with JL DG MOSFETs, given that this is still at its early stage of development [5].

Among the most critical issues regarding short channel effects in JL DG MOSFETs is the drain induced barrier lowering (DIBL) as it affects both static and dynamic operation at low gate voltages. Some works have been done via numerical simulations [6–10], but even though approximate analytical solutions for DIBL in junction based DG MOSFETs [11–17] have been established; only recently some analytical approaches have interestingly been proposed for JL DG MOSFETs. One of them deals with the conformal mapping technique and a decomposition of Poisson's equation into 2D and a 1D part [18,19].

Additional interesting model has been recently derived by solving the 2D Poisson's equation using a variable separation technique which results in expressing the 2D potential distribution through the channel by introducing some series [20].

Another work [21] proposed to solve the potential distribution by splitting the 2D Poisson's equation into a 1D Poisson and 2D Laplace's equations. However, based on this approach, it is still impossible to extract an explicit expression for the subthreshold current and slope.

Lately, Chiang [22] reported an analytical model to calculate the threshold voltage in short channel JL DG MOSFETs assuming a parabolic approximation of the potential across the silicon thickness, but analytical models for subthreshold current, subthreshold slope

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and short channel effects are still missing. In addition, in order to calculate the DIBL, it is usually assumed that the shift in the threshold voltage should equal the shift in the body center potential. We as we will discuss in this paper, we found that such an assumption does not hold anymore in short channel devices.

Given the advantages of using explicit relationships for compact modeling purposes, we propose to derive analytical expressions for the channel potential distribution and related short channel effects in JL DG MOSFET operating below threshold upon technological parameters.

2. Electrostatics in short channel junctionless DG MOSFETS in subthreshold

A schematic view of the *n*-type doped JL DG MOSFET is illustrated in Fig. 1, where L_G and t_{ox} are the gate length and gate oxide thickness, t_{Si} is the semiconductor thickness.

In JL DG MOSFETs, considering a *n*-type doped channel, if the silicon layer is too highly doped and/or too thick, it may be unfeasible to fully deplete the channel from electrons. In this case, a reduction of doping concentration through the channel is needed to achieve suitable threshold voltage and subthreshold slope values. It causes to an increase of source and drain resistance which reduces the *ON* current. It can be corrected by using an additional source and drain implantation [23]. Therefore by considering the $N^+/N/N^+$ doping profile in this study, the doping concentrations for source/drain and channel are $N^+ = 10^{20}\ \mathrm{cm}^{-3}$ and N_D respectively.

The electrostatic potential profile is given from the 2D-Poisson equation:

$$\frac{\partial^2\psi}{\partial x^2}+\frac{\partial^2\psi}{\partial y^2}=\frac{q}{\varepsilon_{si}}\left(n_i e^{\frac{\psi-V}{U_T}}-N_D\right), \tag{1}$$

where *x* and *y* are the orientations along the channel ($0 < x < L_G$) and between the two gates ($0 < y < t_{si}$), *V* and U_T are the electrons quasi Fermi potential and thermal voltage, and n_i and ε_{si} are the intrinsic carrier density and permittivity for silicon.

Since a closed form of (1) is not available and as we are interested in subthreshold operation, we neglect the contribution of mobile charges in (1), leading to:

$$\frac{\partial^2\psi}{\partial x^2}+\frac{\partial^2\psi}{\partial y^2}=-\frac{q}{\varepsilon_{si}}N_D. \tag{2}$$

Next, as suggested by Young [24], we propose to seek for an approximate solution of the 2D potential distribution ($\psi(x,y)$) assuming a parabolic potential along the γ-direction:

$$\psi(x,y)=\psi_s(x)+\varphi_1(x)y+\varphi_2(x)y^2, \tag{3}$$

where $\psi_s(x)$ is the surface potential at $y = 0$ and $y = t_{si}$ (we will consider only symmetric operation). Introducing the symmetric conditions with respect to $t_{si}/2$ gives:

$$\psi(x,y)=\psi_s(x)+\varphi_1(x)y\left(1-\frac{y}{t_{si}}\right). \tag{4}$$

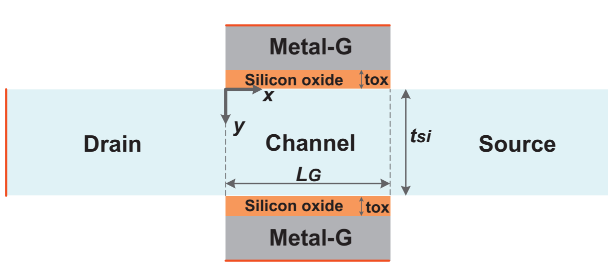

Fig. 1. Schematic view of the *n*-type junctionless DG MOSFET investigated in this work.

In addition, the boundary conditions arising from the continuity of the displacement vector at the silicon–insulator interface must satisfy:

$$\frac{\partial}{\partial y}\psi(x,y)|_{y=0}=\varphi_1(x)=\frac{\varepsilon_{ox}}{t_{ox}\varepsilon_{si}}(\psi_s(x)-V_{GS}+\emptyset_{MS}), \tag{5}$$

where V_{GS} is the gate to source voltage, $\emptyset_{MS}$ is the difference in the work functions between the metal and the semiconductor, t_{ox} is the oxide thickness and ε_{ox} is the oxide permittivity.

Combining (4) and (5), the potential distribution based on the parabolic approximation can be expressed as:

$$\psi(x,y)=\psi_s(x)\left[1+y\left(1-\frac{y}{t_{si}}\right)\frac{\varepsilon_{ox}}{t_{ox}\varepsilon_{si}}\right] + (\emptyset_{MS}-V_{GS})y\left(1-\frac{y}{t_{si}}\right)\frac{\varepsilon_{ox}}{t_{ox}\varepsilon_{si}}. \tag{6}$$

By substituting the above expression in (2), we get a new differential equation in terms of the surface potential ψ_s:

$$\frac{\partial^2}{\partial^2 x}\psi_s(x)-\frac{2\varepsilon_{ox}}{t_{si}t_{ox}\varepsilon_{si}}\psi_s(x)=-\frac{q}{\varepsilon_{si}}N_D+\frac{2\varepsilon_{ox}}{t_{si}t_{ox}\varepsilon_{si}}(\emptyset_{MS}-V_{GS}). \tag{7}$$

From (7) the surface potential along the channel is readily obtained by:

$$\psi_s(x)=\alpha e^{\delta x}+\beta e^{-\delta x}+\gamma, \tag{8}$$

where α and β will be derived later and δ and γ are given by:

$$\delta=\sqrt{2\varepsilon_{ox}/t_{si}t_{ox}\varepsilon_{si}}, \tag{9}$$

$$\gamma=V_{GS}-\emptyset_{MS}+\frac{qN_D}{\delta^2\varepsilon_{si}}. \tag{10}$$

3. Body center potential and limitations of the parabolic approximation in JL DG MOSFET

The principle of operation for junctionless devices is different from the regular junction based double gate device as the current flows through the volume instead of Si–SiO_2 interfaces. From (6) it comes out that, below threshold, the potential at the surface ($y = 0$ and $y = t_{si}$) is lower than at the center ($y = t_{si}/2$) where the electron concentration will peak [5]. Therefore, below threshold, the center of the silicon channel represents the leakiest pathway between the source and the drain, and so DIBL should be modeled regarding the center potential $\psi_{BCP} = \psi(x, t_{si}/2)$.

On the other hand, from (6) the body center potential can be related to surface potential as follows:

$$\psi_{BCP}=\psi(x,t_{si}/2)=a\psi_s(x)+b, \tag{11}$$

where *a* and *b* coefficients are given by:

$$a=1+\frac{1}{8}\delta^2t_{si}^2, \tag{12}$$

$$b=\frac{1}{8}\delta^2t_{si}^2(\emptyset_{MS}-V_{GS}). \tag{13}$$

Here, it is worth noticing that (11) can be used to link the surface to the center potential at any *x* value. As we will argue later, this is quite accurate for gate lengths higher than 30 nm. For gate lengths below 30 nm, the accuracy is slightly degraded but is still acceptable near the center of the channel along the transport direction ($x = L_G/2$), which will be the most relevant region to be investigated. In fact assuming the parabolic approximation for the potential distribution along the *y*-direction as given from (11) generates some mismatch close to the source and drain. Thus, when the gate length is less than 30 nm, we cannot obtain an accurate