



A continuous semi-empiric transfer characteristics model for surrounding gate undoped polysilicon nanowire MOSFETs

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ABSTRACT

A new continuous semi-empiric compact model for the current transfer characteristics of surrounding gate undoped polycrystalline silicon (Poly-Si) nanowire (NW) MOSFETs is proposed. The model consists of a single equation based on the Lambert function, which contains only four parameters and is continuously valid and fully differentiable throughout weak and strong conduction regimes of operation. The model is tested on measured transfer characteristics of experimental devices. The extracted model parameters are used to generate transfer characteristics playbacks that are then compared to the measured data to validate the proposed model's adequacy for these devices.

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1. Introduction

Poly-Si Thin Film Transistors (TFTs) have been receiving a great deal of attention as possible alternatives to amorphous silicon (a-Si) TFTs in several growing application fields. However, the performance of conventional planar Poly-Si TFTs is significantly diminished by the large amount of grain boundary defects in the polysilicon film [1,2] leading to high sub-threshold slope factor and off-state leakage current.

Various technologies continue to be proposed to mitigate the consequences of grain boundaries. Polycrystalline long-channel ultra-thin body surrounding-gate NW MOSFETs have been used for flexible macroelectronics [3] and for highly sensitive biosensor applications [4]. Poly-Si nanowire (NW) channels seem to be promising structures towards alleviating grain boundary effects, because by reducing the NW's cross section the effective number of grain boundaries normal to the direction of current flow can be significantly decreased. Several Poly-Si NW MOSFET structures have been already proposed with that aim [5–8].

Modeling Poly-Si MOSFETs has been a topic of research for many years [2,9,10]. Models for long-channel monocrystalline silicon double- and surrounding-gate MOSFETs also abound [11–15]. In spite of this, we consider that presently available models are still too complex for computationally efficient Poly-Si NW MOSFETs compact modeling applications.

Drain current transfer characteristics compact models have been traditionally assembled following the so called regional approach, in which weak conduction (sub-threshold region) and strong conduction (supra-threshold region) are separately modeled. The resulting regionally valid equations are then mathematically joined near the inter-regional transition (the threshold voltage) by means of arbitrary interpolation (smoothing) functions [16]. On the other hand, the general tendency nowadays aims to the use of continuous (non-regional) models, which do away with the classic threshold voltage parameter, and are continuously differentiable throughout all operation regimes [11].

In what follows we present such a continuous compact model for the drain current transfer characteristics of surrounding gate undoped Poly-Si NW MOSFETs. The model consists of a single Lambert function-based equation that contains only four parameters. It is a semi-empiric model inspired on the general form of the rigorous solutions for the current of hypothetical bulk undoped

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MOSFETs, and on the observed weak and strong conduction behaviors of the experimental devices' transfer characteristics.

The validity of the proposed model is tested on the low drain voltage transfer characteristics of experimental quasi-rectangular section surrounding gate undoped Poly-Si NW MOSFETs of various channel lengths. The model's playbacks, using extracted model parameters, are contrasted against the original measured data.

2. Formulation of the new continuous model

We propose to continuously define the normalized externally applied gate-to-source voltage, V_{GS} , (at low drain-to-source voltage) of Poly-Si NW MOSFETs using a semi-empiric phenomenological description according to the following expressions:

$$\frac{V_{GS} - V_{FB}}{v_{th}} = n \ln \left(\frac{I_D}{I_{oli}} \right) + \left(\frac{I_D}{I_{oh}} \right)^{1/m}, \quad (1a)$$

$$\frac{V_{GS}}{v_{th}} = n \ln \left(\frac{I_D}{I_{ol}} \right) + \left(\frac{I_D}{I_{oh}} \right)^{1/m}, \quad (1b)$$

where I_D is the drain current, $v_{th} = k_B T/q$ is the thermal voltage, V_{FB} is the flat band voltage, I_{oh} is the high conduction parameter, and I_{ol} and I_{oli} are the low conduction parameters which satisfy the following relation: $V_{FB}/v_{th} - n \ln(I_{oli}) = -n \ln(I_{ol})$. It is important to emphasize that the flat band voltage V_{FB} is contained in I_{ol} in Eq. (1b) and accounts for interface traps and work function differences. I_{ol} and I_{oh} are parameters that are drain voltage and geometry dependent, and are given by:

$$I_{ol} = K_l v_{th}^2 \left[1 - \exp \left(-\frac{V_{DS}}{v_{th}} \right) \right] \exp \left(\frac{-V_{FB}}{n v_{th}} \right), \quad (2)$$

$$I_{oh} = K_h v_{th} \zeta V_{DS}, \quad (3)$$

where V_{DS} is the externally applied drain-to-source voltage, K_l and K_h represent channel geometry related transconductance factors (with units of AV^{-2}) at low and high V_{GS} , respectively, which are inversely proportional to channel length L_m [17,18], n is an ideality factor at low voltage, [19,20], and m and ζ are two dimensionless parameters related to the Poly-Si NW MOSFET's mobility dependence on gate bias [21], which will be discussed later. Notice that (1a) and (1b) are continuously valid for any magnitude of drain current (at low drain-to-source voltage), and do not involve any threshold voltage reference to formally separate two regions of weak and strong conduction.

The first term of (1a) corresponds to the carrier transport that prevails at small values of drain current, I_{Dl} , where it is approximately described by:

$$I_{Dl} \approx I_{oli} \exp \left(\frac{V_{GS} - V_{FB}}{n v_{th}} \right) = I_{ol} \exp \left(\frac{V_{GS}}{n v_{th}} \right). \quad (4)$$

On the other hand, the second term of (1a) corresponds to carrier transport at larger drain currents, I_{Dh} , where it may be approximated, at low drain-to-source voltage, by a monomial expression of gate voltage of the form:

$$I_{Dh} \approx I_{oh} \left(\frac{V_{GS} - V_{FB}}{v_{th}} \right)^m = K_h \zeta \left(\frac{V_{GS} - V_{FB}}{v_{th}} \right)^{m-1} (V_{GS} - V_{FB}) V_{DS}. \quad (5)$$

The above monomial equation includes the effect of the Poly-Si nanowire's gate voltage dependent mobility, through the two dimensionless parameters m and ζ . These two parameters arise from empirically expressing the effective mobility, μ_{eff} , as a monomial function of gate voltage, such that:

$$\mu_{eff} \approx \mu_0 \zeta v_{th} \left(\frac{V_{GS} - V_{FB}}{v_{th}} \right)^{m-1}. \quad (6)$$

where μ_0 represents the low field mobility. Here we have implicitly assumed that the mobility exhibits a sub-linear monomial dependence on gate voltage, such that the two dimensionless parameters ζ and m (with m typically < 2) describe that behavior. Eq. (6) corresponds to a reasonable approximate portrayal of the Poly-Si channel's effective mobility enhancement which dominates at moderate values of gate voltage in these Poly-Si NWs. The above formulation is based on a general description of the two main simultaneous mechanisms that fundamentally determine Poly-Si mobility's gate voltage dependence, as expressed by the equation [22,23]:

$$\mu_{eff} \approx \mu_0 \frac{1}{1 + \theta(V_{GS} - V_{FB})} \exp[-s/(V_{GS} - V_{FB})], \quad (7)$$

where θ accounts for the first order gate field degradation mechanism, and s relates to the transport enhancement mechanism brought about by the lowering of grain boundary potential barriers as the applied gate voltage increases.

Solving (1a), (1b) for I_D yields the proposed analytical expression that continuously models the drain current of the undoped Poly-Si NW MOSFET, at low drain voltage:

$$I_D = I_{oli} \times \exp \left\{ \frac{V_{GS} - V_{FB}}{n v_{th}} - m W_0 \left[\frac{1}{mn} \left(\frac{I_{oli}}{I_{oh}} \right)^{1/m} \exp \left(\frac{V_{GS} - V_{FB}}{mn v_{th}} \right) \right] \right\}, \quad (8a)$$

$$I_D = I_{ol} \exp \left\{ \frac{V_{GS}}{n v_{th}} - m W_0 \left[\frac{1}{mn} \left(\frac{I_{ol}}{I_{oh}} \right)^{1/m} \exp \left(\frac{V_{GS}}{mn v_{th}} \right) \right] \right\}, \quad (8b)$$

where W_0 stands for the short hand notation of Lambert function's principal branch [24]. The above transfer characteristics model exhibits the same general kind of gate voltage functional form as the channel charge [25], the drain current of undoped crystalline MOSFETs [26], or the surface potential in crystalline undoped nanowire MOSFETs with Schottky-Barrier source/drain [27]. We wish to emphasize that the model represented by (8a), (8b) does not contain any interpolation or smoothing function, which in a regional type of model would be needed to join sub-threshold (weak conduction) and supra-threshold (strong conduction) current equations about some threshold voltage reference, which does not explicitly exist in this model.

It might be noted that the first term ($V_{GS}/n v_{th}$) of the exponential's argument in (8b) dominates over the second term ($m W_0(\dots)$) at low values of gate voltage, where the latter is still negligible with respect to the former. The second term, which subtracts from the first, becomes increasingly dominant as the gate voltage increases, and finally determines the overall behavior in strong conduction.

It is also worth observing that not only is this model a continuous function of gate voltage, but its derivatives are also continuous. Thus, the device's transconductance can be conveniently modeled by an explicit and continuous function of gate voltage:

$$g_m = \frac{I_{ol} \exp \left(\frac{V_{GS}}{n v_{th}} \right) \exp \left\{ -m W_0 \left[\frac{1}{mn} \left(\frac{I_{ol}}{I_{oh}} \right)^{1/m} \exp \left(\frac{V_{GS}}{mn v_{th}} \right) \right] \right\}}{n v_{th} \left\{ 1 + W_0 \left[\frac{1}{mn} \left(\frac{I_{ol}}{I_{oh}} \right)^{1/m} \exp \left(\frac{V_{GS}}{mn v_{th}} \right) \right] \right\}}. \quad (9)$$

Furthermore, the transconductance-to-current ratio may be expressed also as an explicit function of gate voltage:

$$g_m/I_D = \frac{\left\{ 1 + W_0 \left[\frac{1}{mn} \left(\frac{I_{ol}}{I_{oh}} \right)^{1/m} \exp \left(\frac{V_{GS}}{mn v_{th}} \right) \right] \right\}^{-1}}{n v_{th}}. \quad (10)$$

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