Solid-State Electronics 63 (2011) 149–153

Contents lists available at ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

Scattering parameter based modeling and simulation of symmetric tied-gate InAlAs/InGaAs DG-HEMT for millimeter-wave applications

Monika Bhattacharya [a], Jyotika Jogi [b], R.S. Gupta [c], Mridula Gupta [a,*]

[a] Semiconductor Device Research Laboratory, Department of Electronic Science, University of Delhi, South Campus, New Delhi 110 021, India
[b] Department of Electronic Science, A.R.S.D. College, University of Delhi, South Campus, New Delhi 110 021, India
[c] Department of Electronics and Communication Engineering, Maharaja Agrasen Institute of Technology, Sector-22, Rohini, New Delhi 110 086, India

ARTICLE INFO

Article history:
Received 18 February 2011
Received in revised form 24 May 2011
Accepted 30 May 2011
Available online 5 July 2011

The review of this paper was arranged by Prof. A. Zaslavsky

Keywords:
Double-gate HEMT
Symmetric
Tied-gate
Small-signal equivalent circuit
Scattering parameters
Unilateral Transducer Power Gain

ABSTRACT

This paper analyses the RF performance of the symmetric tied-gate $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ DG-HEMT in terms of its maximum frequency of oscillation (f_{max}) and the other important figures of merit that include Maximum Unilateral Transducer Power Gain and the Maximum Stable Gain. This comprehensive investigation has been done on the basis of scattering parameters in order to judge the potential of InAlAs/InGaAs DG-HEMT as the device for future millimeter wave frequency applications. The effect of parasitic elements has also been included in the analytical model which leads to better correspondence with the experimental results. The analytical results thus obtained using the charge control model are compared and found to agree well with both the ATLAS-3D device simulation results as well as the experimental results.

1. Introduction

The state-of-the art RF performance exhibited by the sub 100 nm gate-length InGaAs channel DG-HEMTs during the past few decades has ensured continued interest and steered extensive research for further exploration of the potential of this highly promising device for future military communications, radar and intelligence applications [1]. Superior ultra-high frequency and low-noise performance reported for the 100 nm gate-length trenched gate InAlAs/InGaAs DGHEMT fabricated via the transferred substrate technique [2] has provided great motivation to develop an accurate analytical ac model which enables rigorous RF performance assessment of the device and also forms the basis for the modeling of its noise performance [3–5]. The authors had proposed a charge control based model for the symmetric tied-gate $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ DG-HEMT establishing the enhanced microwave performance vis-à-vis its single-gate counterpart. The results obtained were shown to agree well with the experimental results earlier reported [4,5].

The present analysis begins with obtaining the intrinsic short-circuit admittance (y) parameters of the device in terms of the various elements of its two-port intrinsic small-signal equivalent circuit (SSEC) followed by its conversion into scattering parameters also including the effect of the various parasitic elements. The scattering parameter analysis of the device which is very vital for a comprehensive analysis of the ultrahigh frequency performance yields relevant figures of merit that includes Maximum Unilateral Power Gain (G_{tumax}), Maximum Stable Gain (G_{ms}) and the maximum frequency of oscillation (f_{max}). The model thus established enables complete microwave characterization of the device for the millimeter wave low-noise amplifier design applications.

2. Model formulation

A symmetric tied gate $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ DG-HEMT shown in Fig. 1 leads to the reduction of the equivalent 3-port network to a simplified 2-port equivalent circuit which is then mathematically analyzed for the extraction of its various small signal parameters.

Using the proposed charge control model, the sheet carrier concentration in the 2DEG is given as [6–8]:

* Corresponding author. Tel.: +91 11 24115580; fax: +91 11 24110606.
E-mail addresses: monika.bhattacharya86@gmail.com (M. Bhattacharya), jogijyotika@arsd.du.ac.in (J. Jogi), rsgu@bol.net.in (R.S. Gupta), mridula@south.du.ac.in (M. Gupta).

0038-1101/$ - see front matter © 2011 Elsevier Ltd. All rights reserved.
doi:10.1016/j.sse.2011.05.025

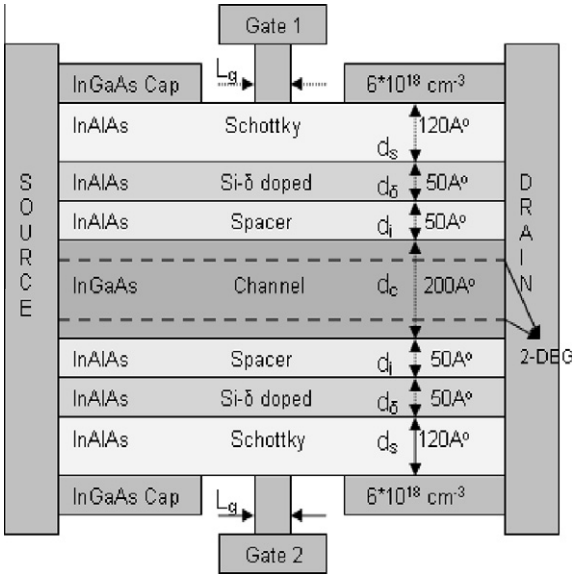

Fig. 1. Schematic of symmetric tied gate InAlAs/InGaAs DG-HEMT.

$$n_s(x) = n_{so}\left\{\alpha + (1-\alpha)\tanh\left[\frac{(V_{gs} - V_{gm} - V_c(x))}{V_1}\right]\right\} \tag{1}$$

and the maximum 2DEG concentration is:

$$n_{so} = \left[\left(\frac{2\varepsilon_d N_d}{q}\right)\left(\Delta E_c - \Delta E_f + \Delta E_{f1} + \frac{k\cdot T}{q}\right) + N_d^2(d+\Delta d)^2\right]^{\frac{1}{2}} - N_d(d+\Delta d) \tag{2}$$

In the above equation, q is the electron charge, k is the Boltzmann constant, the permittivity of $In_{0.53}Ga_{0.47}As$ is $\varepsilon_d = 12.47\varepsilon_o$, where, ε_o is the absolute permittivity of free space, μ_o is the electron mobility (0.83 m^2/V-s), $d = d_d + d_i$ is the total thickness of the InAlAs layer where $d_d = d_s + d_a$, Δd is the distance of the 2DEG from the heterointerface (~60 Å), ΔE_c (0.52 eV) is the conduction-band discontinuity at the InAlAs/InGaAs interface, ΔE_f is the position of the fermi-level below the bottom of the conduction-band (~0 eV at 300 K), ΔE_{f1} is the small energy arising from the linear approximation of n_s vs fermi-level (~0 eV at 300 K) and N_d is the donor concentration of the δ-doped layer ($\sim 0.25 \times 10^{25}$ m^{-3}). v_{sat} is the saturation velocity (2.63×10^5 m/s).$V_c(x)$ is the potential in the channel with α, V_{gm}, V_1 as the three fitting parameters [6]. The dimensions of various layers are shown in Fig. 1 with gate-length $L_g = 100$ nm and channel width $Z = 100$ μm.

Using (1) and (2), the net drain to source current is given as [6]:

$$I_{ds} = \frac{\frac{2\cdot q\cdot Z\cdot n_{so}\cdot \mu_o}{L_g}[X]}{1 + \frac{\mu_o \cdot V_{ds}}{L_g \cdot v_{sat}}} \tag{3}$$

where,

$$X = \frac{(1-\alpha)\cdot V_1}{2}(X_1 - X_o) \tag{4}$$

$$X_o = \ln(y_o^2 - 2\cdot\alpha\cdot y_o + (2\cdot\alpha - 1)) + \frac{\alpha}{(1-\alpha)} \times \ln\left(\frac{y_o - 1}{y_o - 2\cdot\alpha + 1}\right) \tag{5}$$

$$X_1 = \ln(y_1^2 - 2\cdot\alpha\cdot y_1 + (2\cdot\alpha - 1)) + \frac{\alpha}{(1-\alpha)} \times \ln\left(\frac{y_1 - 1}{y_1 - 2\cdot\alpha + 1}\right) \tag{6}$$

$$y_o = \left[\alpha + (1-\alpha)\tanh\left(\frac{V_{gs} - V_{gm}}{V_1}\right)\right]; \quad y_1 = \left[\alpha + (1-\alpha)\tanh\left(\frac{V_{gs} - V_{gm} - V_{ds}}{V_1}\right)\right] \tag{7}$$

Fig. 2 exhibits the dc behavior of the device which is in good agreement with the experimental results. The intrinsic small signal equivalent circuit (SSEC) of InAlAs/InGaAs DG-HEMT is shown in Fig. 3. The physical significance and the values of the extrinsic elements are given in Table 1 [4,9].

The *transconductance* (g_m) *and drain Conductance* (g_d) which govern the intrinsic gain of the device (g_m/g_d) are obtained using (3). The gate-capacitances including *gate-source capacitance* (C_{gs}) *and gate-drain capacitance* (C_{gd}) are obtained using (1). The cut-off frequency which determines the ultimate speed of the device is obtained using $f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})}$. For short channel devices we can approximate the time constant $R_i \cdot C_{gs}$ as the transit time of the car-

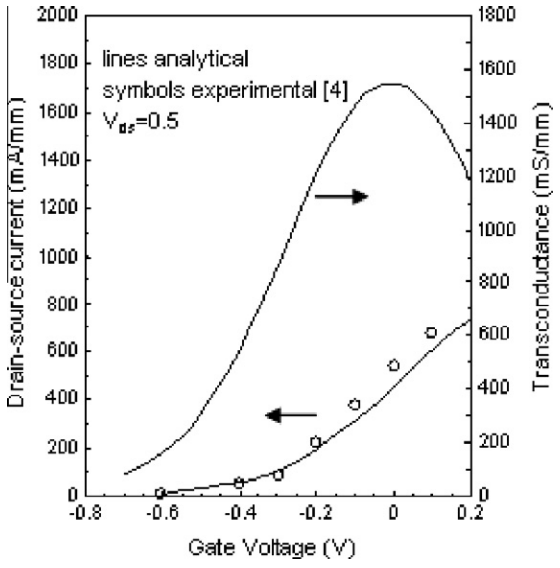

Fig. 2. Variation of drain current and transconductance with gate voltage.

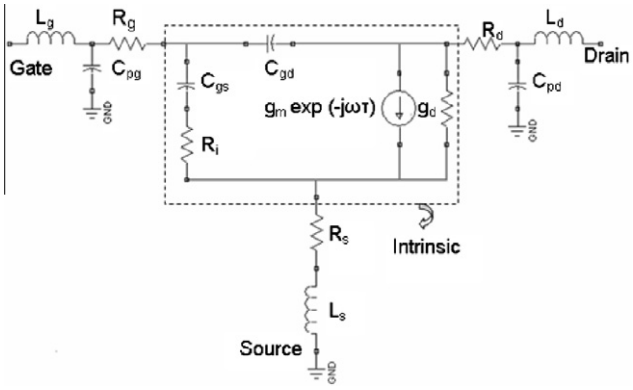

Fig. 3. SSEC of tied-gate InAlAs/InGaAs DG-HEMT.