Solid-State Electronics 63 (2011) 163–166

Contents lists available at ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

Charge carrier injection and transport associated with thermally generated cracks in a 6,13-bis(triisopropylsilylethynyl) pentacene thin-film transistor

Jin-Hyuk Bae [a,1], Hyeok Kim [b], Gilles Horowitz [b], Sin-Doo Lee [a,*]

[a] School of Electrical Engineering #32, Seoul National University, Kwanak P.O. Box 34, Seoul 151-600, Republic of Korea
[b] ITODYS, Université Paris Diderot (Paris 7), CNRS, 75205 Paris, France

ARTICLE INFO

Article history:
Received 2 March 2011
Received in revised form 19 April 2011
Accepted 18 May 2011
Available online 12 June 2011

The review of this paper was arranged by Prof. S. Cristoloveanu

Keywords:
Crack
TIPS-pentacene
Post-thermal annealing
Carrier injection
Carrier transport
Interfacial resistance

ABSTRACT

We describe how the charge carrier injection and transport are influenced by thermal cracks in a 6,13-bis(triisopropylsilylethynyl) (TIPS) pentacene film in terms of the contact resistance and the channel resistance in a TIPS pentacene thin-film transistor (TFT). Through a post-thermal annealing (PTA) process at a certain temperature T_a, the high structural order of TIPS-pentacene molecules is produced without thermal cracks, the carrier mobility of the TIPS pentacene TFT is maximized, and both the contact resistance and the channel resistance are minimized. Our quantitative description of the relationship between the PTA treatment and the interfacial resistance behavior would provide a useful basis for understanding the thermal stability and the electrical performance of a solution-processed organic TFT.

1. Introduction

Recently, organic thin-film transistors (OTFTs) have attracted much attention from several advantages such as the mechanical flexibility, the low-temperature processing capability at low cost, and the applicability to plastic substrates [1–4] over conventional silicon-based driving elements. In contrast to many of the OTFTs that suffer generally from poor electrical properties, for example, low current on–off ratio and low charge carrier mobility [5,6], pentacene-based TFTs fabricated by vacuum-deposition have shown the carrier mobility comparable to the level of amorphous silicon [7–9]. For large-area, low-cost applications, it is desirable to develop solution-processing organic semiconductors, one of which is 6,13-bis(triisopropylsilylethynyl) (TIPS) pentacene [10–12]. In such TIPS pentacene, however, the development of thermal cracks was found to be one of the critical problems to be solved [13–15]. Furthermore, it is necessary to investigate the effect of the thermal cracks on both the charge injection through an organic semiconductor layer interfaced with a metal electrode and the charge transport at an organic semiconductor–gate insulator interface.

In this work, we describe how the charge carrier injection and transport are influenced by thermal cracks generated in a 6,13-bis(triisopropylsilylethynyl) (TIPS) pentacene film in terms of the contact resistance and the channel resistance in a TIPS pentacene thin-film transistor (TFT). Through a post-thermal annealing (PTA) process at a certain temperature T_a, the highest crystallinity in a TIPS pentacene film was obtained without thermal cracks, and both the contact resistance and the channel resistance in a TIPS pentacene TFT were minimized. As the PTA temperature was increased above T_a, the cracks were found to be developed due to the side-chains in the TIPS pentacene molecules and the carrier mobility was significantly decreased [14]. Thus, it is very important to determine the interfacial resistance of a TIPS pentacene TFT in relation to the thermal cracks in a TIPS pentacene film for acquiring the electrical and thermal stabilities of solution-processed OTFTs.

2. Experimental

A bottom gate, top contact pentacene TFT used in our study was shown in Fig. 1. An indium–tin-oxide (ITO) layer on a glass substrate was used as a gate electrode. The ITO patterned substrate was cleaned with acetone, isopropyl alcohol, methyl alcohol, and de-ionized water in sequence. A gate insulator of poly(4-vinylphe-

* Corresponding author. Tel.: +82 2 880 1823; fax: +82 2 874 9769.
E-mail address: sidlee@plaza.snu.ac.kr (S.-D. Lee).
[1] Present address: Department of Bioelectronics, Provence Microelectronics Centre, Ecole Nationale Supérieure des Mines de Saint-Etienne, Gardanne 13541, France.

0038-1101/$ - see front matter © 2011 Elsevier Ltd. All rights reserved.
doi:10.1016/j.sse.2011.05.014

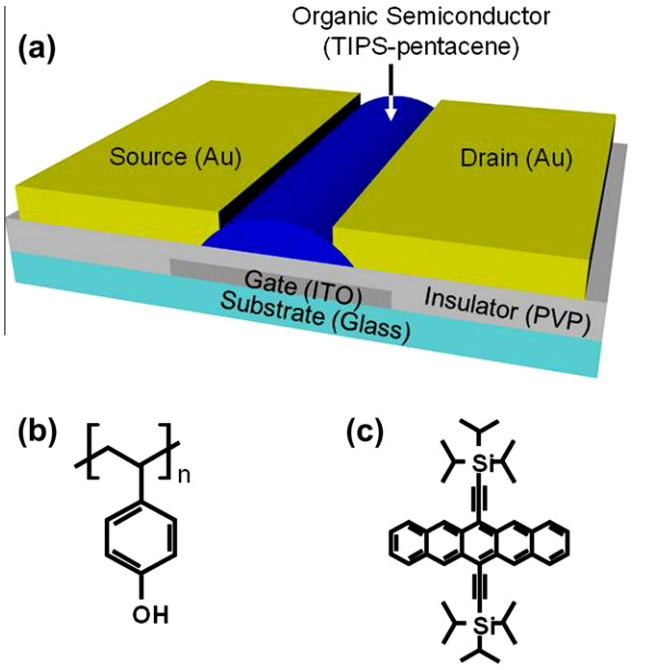

Fig. 1. (a) The schematic diagram of a bottom gate, top contact TIPS pentacene TFT with a PVP gate insulator. The chemical structures of (b) the PVP and (c) the TIPS pentacene.

nol) (PVP) mixed with a thermal cross-linking agent methylated poly(melamine-co-formaldehyde) (MMF) in 125 wt.% was prepared as described previously [16].

The PVP with MMF was dissolved in propylene glycol methyl ether acetate (PGMEA) in 10 wt.% and then spin-coated on the ITO patterned substrate. The spin-coated PVP layer was baked at 100 °C for 1 min to remove any residual PGMEA, and subsequently baked for 5 min at 200 °C to promote thermal cross-linking in the PVP layer [14]. The thickness and the capacitance per unit area of the cross-linked PVP layer were about 550 nm and 6.52 nF/cm^2, respectively. An active layer was produced from a solution of the TIPS pentacene in 1.0 wt.% in 1,2-dicholorobenzene on the PVP insulator by drop-casting and cured at 60 °C for 1 min on a hotplate at ambient condition to evaporate the solvent. Note that the PVP gate insulator is chemically inert against the solvent of the TIPS pentacene, 1,2-dicholorobenzene. The source and drain electrodes of Au were deposited on the TIPS pentacene film through a shadow mask at the deposition rate of 1 Å/s. The thickness of Au was 80 nm. The channel length (L) in our TIPS pentacene TFTs was varied from 50 to 120 μm while the channel width (W) was fixed to be 2 mm. For completely fabricated TIPS pentacene TFTs, the PTA processes at two different temperatures, one of which was 60 °C (T_a) and the other was 150 °C (above T_a), were carried out under ambient condition for 3 h. Note that thermal cracks were developed in the TIPS pentacene through the PTA process above T_a [14]. The electrical performance of the TIPS pentacene TFTs was measured using a semiconductor parameter analyzer (HP4155A) at room temperature (RT) under ambient pressure.

3. Results and discussion

We first examine the crack development at the interface between the TIPS pentacene film and the Au electrode by the PTA treatment. It is clear that no cracks were appeared in the TIPS pentacene films with no PTA process in Fig. 2a and the PTA treatment at 60 °C in Fig. 2b. The PTA treatment below 60 °C did not

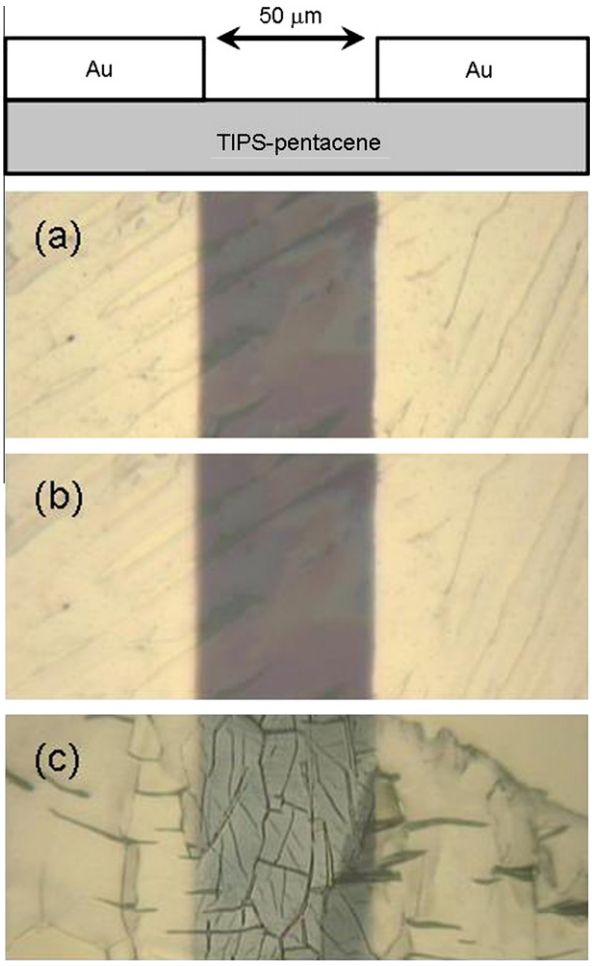

Fig. 2. The optical microscopic images of TIPS pentacene films where patterned Au electrodes were deposited. TIPS pentacene film with no PTA process is shown in (a). TIPS pentacene films with the PTA treatment at (b) 60 °C and (c) 150 °C. The gap between two Au electrodes represents the channel length of 50 μm in the TIPS pentacene OTFT.

produce any thermal crack at a gate insulator-TIPS pentacene interface as observed previously [13,15]. Note that in the TIPS pentacene film, the cracks become appeared just above 60 °C and grown with increasing the annealing temperature. As shown in Fig. 2c, the cracks were substantially developed over the whole area in the TIPS pentacene film treated at 150 °C.

Let us examine the effect of the thermally developed cracks on the magnitude of the mobility in the TIPS pentacene OTFT. Fig. 3a show the transfer characteristic curves of our three types of the OTFTs; the first type with no PTA process, the second type with the PTA treatment at 60 °C (represented by region I below T_a), and the third type with the PTA treatment at 150 °C (represented by region II above T_a). The drain current I_D was measured at the drain voltage V_D of −40 V as a function of the gate voltage V_G. The carrier mobility in the saturation region (μ_{sat}) was determined from the characteristic curve using the following equation [17]:

$$\mu_{sat} = \frac{2L}{W \cdot C_i} \cdot \frac{I_D}{(V_G - V_T)^2},$$

where I_D is the drain current, C_i is the capacitance of the gate insulator, and V_T is the threshold voltage. At fixed voltage of $V_D = V_G = -40$ V, the carrier mobility μ_{sat} is 0.15 cm^2/Vs for the as-prepared OTFT, 0.36 cm^2/Vs for the OTFT with the PTA treatment at 60 °C, and 0.05 cm^2/Vs for the OTFT with the PTA treatment at