Solid-State Electronics 60 (2011) 70–74

Contents lists available at ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

Control of interfacial properties of Pr-oxide/Ge gate stack structure by introduction of nitrogen

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ARTICLE INFO

Article history:
Available online 22 February 2011

Keywords:
Ge
Pr-oxide
Radical nitridation
Interface state density

ABSTRACT

We have demonstrated the control of interfacial properties of Pr-oxide/Ge gate stack structure by the introduction of nitrogen. From *C–V* characteristics of Al/Pr-oxide/Ge_3N_4/Ge MOS capacitors, the interface state density decreases without the change of the accumulation capacitance after annealing. The TEM and TED measurements reveal that the crystallization of Pr-oxide is enhanced with annealing and the columnar structure of cubic-Pr_2O_3 is formed after annealing. From the depth profiles measured using XPS with Ar sputtering for the Pr-oxide/Ge_3N_4/Ge stack structure, the increase in the Ge component is not observed in a Pr-oxide film and near the interface between a Pr-oxide film and a Ge substrate. In addition, the N component segregates near the interface region, amorphous Pr-oxynitride (PrON) is formed at the interface. As a result, Pr-oxide/PrON/Ge stacked structure without the Ge-oxynitride interlayer is formed.

1. Introduction

Germanium (Ge) is an attractive candidate for a channel material of the future high-speed metal–oxide-semiconductor field effect transistor (MOSFET) because of its high-mobility of both electrons and holes compared to silicon (Si) [1,2]. In addition, Ge is a promising material for a low operation power devices because its small energy bandgap. On the other hand, rare-earth metal oxides with high dielectric constant more than 30 have attentions as an alternative candidate to Hf-based high dielectric constant (high-*k*) gate dielectrics in the next generation MOSFET devices [3,4].

However, there are some problems about the interfacial structure between a rare-earth high-*k* insulator and a Ge channel and its electrical properties. The first one is the formation of a Ge-oxide (GeO_x) interlayer with a low dielectric constant ($\varepsilon_r \sim 6$) during the deposition of high-*k* films and the thermal treatment [5]. There is an attractive aspect in GeO_2/Ge interfacial structure, which can realize the very low interface state density lower than 10^{11} eV^{-1} cm^{-2} [6–8]. However, the formation of a thin GeO_2 interlayer is difficult because of the active reaction between Ge and oxygen. That is not suitable for the equivalent oxide thickness (EOT) scaling. Furthermore, the second problem is that the increase in the interface state density is caused with the desorption of GeO from the GeO_2/Ge interface [9,10]. The GeO desorption from the interface occurs mainly with the thermal annealing treatment, and it becomes more severe when the thicknesses of the GeO_2 interlayer and high-*k* dielectrics become thinner. Actually, it is reported that the interface state density increases with decreasing in the thickness of GeO_2 interlayers [11]. The third is the reduction of the dielectric constant of high-*k* films due to the diffusion of Ge into high-*k* films from Ge channel [5,12,13]. Therefore, we have to control the stability of the high-*k*/Ge interfacial structure and its electrical properties in order to realize both a lower interface state density and a higher thermal robustness without a thick interface control layer.

Ge-nitride (Ge_3N_4) is a promising material as an interfacial layer to control interfacial properties between a high-*k* layer and a Ge channel, because its thermal decomposition temperature is generally higher than GeO_2 [14,15]. In addition, it is possible to realize the no-oxygen interfacial structure using a Ge_3N_4 interlayer and to suppress the formation of a GeO_x interlayer. Furthermore, the introduction of nitrogen (N) into the high-*k*/Ge interface is also attractive to control interfacial properties, since there are some reports that the interface state densities of HfO_2/Ge(O)N/Ge and praseodymium (Pr)-oxide/PrON/Ge stacked structure decrease after annealing [16–18]. In addition, Kutsuki et al. reported that a Ge-nitride capping layer is effective for the preservation of the GeO_2/Ge interlayer and the reduction of the leakage current [19]. However, the improvement effect of N on high-*k*/Ge interfacial properties has not been clarified yet, and the distribution of N in high-*k*/nitride/Ge stack structures has not been optimized. Furthermore, rare-earth high-*k* dielectrics are more hopeful materials to the EOT scaling since a dielectric constant of a nitride interlayer is not so high. In this study, we focus on Pr-oxide films. Pr-oxide has a very high bulk dielectric constant ($\varepsilon_r \sim 31$), and a small leakage current due to f-electrons in a narrow sub-band with the heavy effective mass [20–24]. However, Pr-oxide has some valence values such as Pr^{3+} and Pr^{4+} in an oxide film [20,21,24–26]. This phenomenon leads to the formation of oxide traps due to the lack of oxygen (oxygen

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0038-1101/$ - see front matter © 2011 Elsevier Ltd. All rights reserved.
doi:10.1016/j.sse.2011.01.029

vacancy). In addition, an excess oxygen supplied from a Pr-oxide to the interface may also cause the unexpected formation of a GeO_x interlayer at the Pr-oxide/Ge interface.

In this study, we investigated electrical properties and chemical bonding states of Pr-oxide/Ge_3N_4/Ge stacked structure. Ge_3N_4 films were formed using the radical nitridation technique [18]. The radical nitridation technique is a strategic method to prepare nitride films on Ge devices at a low temperature, because activation species with the high internal energy are used. On the other hand, Pr-oxide films were deposited by the atomic layer deposition (ALD) method using $Pr(EtCp)_3$ precursor to control the film thickness and its fluctuation [25].

2. Experimental

P-type Ge(0 0 1) wafers with a resistivity of 1.0–5.0 Ω cm were used. After the chemical cleaning using 2%-diluted-HF solution and de-ionized water, substrates were set in an ultra-high vacuum chamber with a base pressure below 4×10^{-7} Pa. A 1 nm-thick Ge_3N_4 thin layer was formed at 300 °C using the radical nitridation technique. Nitrogen radicals were formed using an inductively-coupled-plasma (ICP) source with a RF power of 500 W and a partial pressure of nitrogen gas (N_2) of 4×10^{-3} Pa. Then, a Pr-oxide film was deposited using ALD method (Picosun SUNALE R-150B) at the temperature range of 130 and 150 °C. $Pr(EtCp)_3$ and H_2O were used as an precursor. The thickness of Pr-oxide films were ranging from 4 to 8 nm. Aluminum (Al) gate and back electrodes with the area of 1.3×10^{-4} cm^2 for MOS capacitors were fabricated with the vacuum deposition. Finally, some samples were annealed at 300 °C for 30 min in H_2 ambient.

The chemical bonding state of Pr-oxide/Ge_3N_4/Ge stacked structures were characterized with X-ray photoelectron spectroscopy (XPS) using the Mg Kα line ($h\nu$ = 1253.6 eV). The depth profiles of component elements were evaluated from an area intensity of XPS spectra with argon ion (Ar^+) sputtering. We also measured capacitance–voltage (*C–V*) and leakage current characteristics of MOS capacitors at a temperature ranging from 170 K to room temperature. The interface state density was evaluated using the conductance method at a low temperature.

3. Results and discussion

Fig. 1a and b show *C–V* characteristics of (a) Al/Pr-oxide/Ge and (b) Al/Pr-oxide/Ge_3N_4/Ge [18] MOS capacitors. The measurement temperature and frequency are 190 K and 1 MHz, respectively. The formation temperatures of Pr-oxide layers are (a) 130 °C and (b) 150 °C. The accumulation capacitance of the Al/Pr-oxide/Ge sample without a nitride interlayer obviously decreases after annealing. In addition, *C–V* characteristic of this sample degrades with annealing. On the other hand, there is no reduction of the accumulation capacitance of the Al/Pr-oxide/Ge_3N_4/Ge sample even after annealing. This result indicates that the nitride interfacial layer effectively suppresses the formation of a Ge-oxide (GeO_x) interlayer with a low dielectric constant ($\varepsilon_r \sim 6$) and the diffusion of Ge into Pr-oxide during annealing. The details of the dielectric constant of Pr-oxide films will be discussed later. In addition, the *C–V* characteristic of the annealed Al/Pr-oxide/Ge_3N_4/Ge sample is obviously improved compared to that before annealing. This result suggests the decrease in the interface state density after annealing.

Fig. 2 shows the interface state density of Al/Pr-oxide/Ge and Al/Pr-oxide/Ge_3N_4/Ge MOS capacitors as a function of the surface potential. The interface state density was measured using the conductance method at the temperature ranging from 170 K to room temperature. In the sample after annealing without nitride interlayer, the interface state density is too large to estimate using conductance method, although that of the sample before annealing is relatively small. From also this result, it is found that the electrical properties of Al/Pr-oxide/Ge sample degrade after annealing. On the other hand, the interface state density of the Al/Pr-oxide/Ge_3N_4/Ge sample decreases by more than one order magnitude after annealing as shown in Fig. 1a. In this study, we achieve the interface state density as low as 3.5×10^{11} eV^{-1} cm^{-2}. Here, we consider that this interface state is related to defects formed just at the interface between the oxide film and the Ge substrate. On the other hand, we can certainly find the hysteresis in *C–V* properties. This indicates the existence of the slow trap near the interface in oxide films, although the origin of this trap is different from that of the interface state. The density of slow oxide trap is evaluated to be 2×10^{12} cm^{-2} from the hysteresis width of the *C–V* curve.

Fig. 3 shows the leakage current properties of the Al/Pr-oxide/PrON/Ge samples before and after H_2 annealing. The gate voltage is negative and it is the accumulation condition of MOS capacitors. We can achieve the leakage current densities as low as 10^{-9} A/cm^2 order at the gate voltage of higher than −2 V for the sample before and after H_2 annealing.

Fig. 4a–h show cross-sectional TEM images and TED patterns of Pr-oxide/Ge and Pr-oxide/Ge_3N_4/Ge stacked structures. At first, an increase in the thickness of Pr-oxide and GeO_x interlayer are not observed after annealing in both samples. On the other hand, the local crystallization is observed before annealing in both samples.

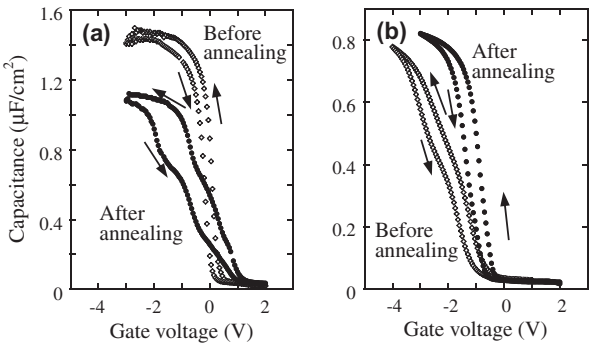

Fig. 1. *C–V* characteristics measured at 190 K of (a) Al/Pr-oxide/Ge and (b) Al/Pr-oxide/Ge_3N_4/Ge MOS capacitors before and after annealing. Oxide thicknesses in Al/Pr-oxide/Ge MOS capacitors before and after H_2 annealing are 4.3 and 4.1 nm. Insulator thicknesses in Al/Pr-oxide/Ge_3N_4/Ge MOS capacitors before and after H_2 annealing are 8.5 and 8.0 nm, respectively.

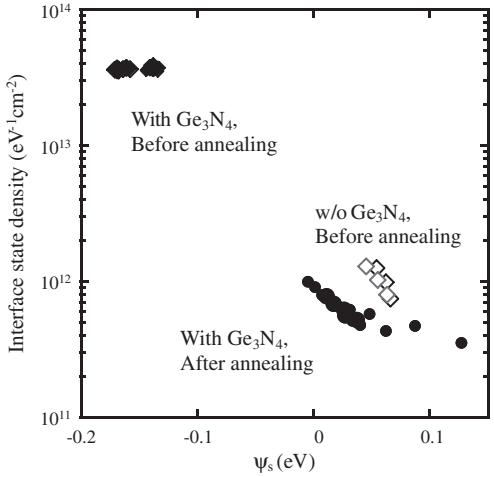

Fig. 2. Interface state density as a function of surface potential for Al/Pr-oxide/Ge and Al/Pr-oxide/Ge_3N_4/Ge MOS capacitors.