



Introduction of local tensile strain on Ge substrates by SiGe stressors selectively grown on wet chemically recessed regions for strained Ge-*n*MOSFETs

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ABSTRACT

Introduction of tensile strain into Ge substrates was demonstrated by forming embedded SiGe stressors on the recessed regions formed by an anisotropic wet chemical etching process for strained Ge-*n*MOSFETs having high electron mobility. A damage-free and well controlled anisotropic wet chemical etching process is developed in order to avoid plasma-induced damages in a conventional RIE process. The uni-axial tensile strain over 1% near the Ge recess-edge regions, which is induced by the embedded SiGe stressors, is also demonstrated for the first time. These results suggest that higher electron mobility than the upper-limit for a Si-MOSFET is obtainable in short channel strained Ge-*n*MOSFETs with the embedded SiGe stressors.

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1. Introduction

Introduction of strain to channels has become a mature technology for high drive current by enhancing the carrier mobility in Si-CMOS devices [1,2]. As for *n*MOSFETs, the electron mobility in strained Si channels, however, is limited up to around twice of that of unstrained Si channels [3]. It has been theoretically reported, on the other hand, that superior electron mobility up to around 4 times of the value of unstrained Si channels, which corresponds to twice of that in tensile strained Si channels, can be realized in Ge channels, by applying tensile strain around 1% or higher to Ge channels [4]. The tensile strain is expected to be applied by SiGe S/D stressors adjacent to the Ge channel region as shown in Fig. 1, which can be formed with Selective Epitaxial Growth (SEG) as Si:C S/D stressors are utilized for tensile strained Si channels [2]. Diode characteristics fabricated in strained SiGe layers on Ge substrates also suggest additional advantages of SiGe S/D stressors such as better short channel characteristics by a smaller diffusion coefficient of P-dopants and lower BTBT leakage currents due to the wider band gap of SiGe than that of Ge [5]. However, the tensile strain in Ge channels with SiGe stressors have not been observed yet. This may be attributable to a significantly lower yield stress and faster dislocation velocity in Ge than in Si, which can be origins of strain relaxation due to a plastic deformation around the stressed Ge channels [6]. In this paper, observation of the tensile strain on Ge substrates by embedded SiGe stressors is dem-

onstrated for the first time. A damage-free and well controlled anisotropic wet chemical etching is also demonstrated to form the recessed region for the SiGe stressor growth in order to avoid plasma-induced damages in a conventional RIE process.

2. Experimental

Experimental details about Ge recess formation and SiGe stressor SEG are shown as follows. First, a CVD-grown SiO₂ dummy gate layer was patterned into *L*(Line)/*S*(Space) (= 0.6/1.4 μm) in parallel with a [0 1 1] direction on a Ge(1 0 0) substrate. Subsequently, 50 nm-depth recess structures were anisotropically etched on the exposed Ge surfaces with HF + H₂O₂ solution [7]. 70 nm-thick embedded SiGe stressor layers with the Ge composition, *x*, of 0.7, 0.8 and 0.9 were selectively grown on the recessed region in a hot-wall LP-CVD chamber using SiH₄ and GeH₄. The growth temperature and pressure were 450 °C and 1 Pa, respectively. The Ge composition of these samples was determined with XRD. The structures were observed with SEM and TEM. The strain applied in the Ge layers was measured with micro-Raman spectroscopy.

3. Results and discussion

3.1. Recess formation with anisotropic wet etching

First, the wet etchant for Ge recess etching was optimized to minimize the undercut beneath the dummy-gate. This is necessary to control the alignment of the SiGe stressors against the gate stack and the sidewalls of the MOSFET. Here, anisotropic wet etching, in

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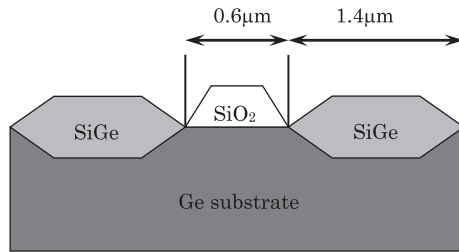


Fig. 1. Schematic cross-sectional view of the fabricated strained Ge structure with embedded SiGe stressors.

which the etching rate of Ge(1 1 1) planes is the lowest, is suitable to minimize the undercut region. Moreover, it is considered that process-induced damages in Ge can be suppressed with the wet etching, unlikely with conventional RIE processes. A SEM images of the etched region, which was both defined by (1 1 1) and (1 0 0) planes, after etching with the HF + H₂O₂ solution and H₂O₂ solution are shown in Fig. 2 [8]. A ratio of the etching depth, D , to the undercut, W , of around 10 was obtained under the opti-

mized condition for the HF + H₂O₂ solution, although that of at most 4 was obtained with the H₂O₂ etching. Here, the reason of the enhancement of the anisotropy is considered to be attributable to the lower pH of the HF + H₂O₂ etchant than that of H₂O₂ solution, due to the addition of HF in consideration of Pourbaix diagram of Ge [9].

3.2. Selective epitaxial growth of SiGe stressors

Next, SiGe SEG was applied on the recessed regions using only hydride source gases without etching gas, which is usually employed for SEG processes. This method can be advantageous to avoid crystal defect generation during the film growth as well as to keep high throughput because higher growth rate is obtainable at lower growth temperatures than in a conventional SEG process using etching gas. It is, on the other hand, still not clear that SEG without using etching gas can be realized at low temperatures in a hot-wall CVD chamber, because hydride source gases are cracked not only on the surfaces but also on the wall of the CVD chamber, resulting in physical deposition of Si or Ge atoms on the surfaces. As a result, Ge-rich SiGe layers having flat surfaces with x down

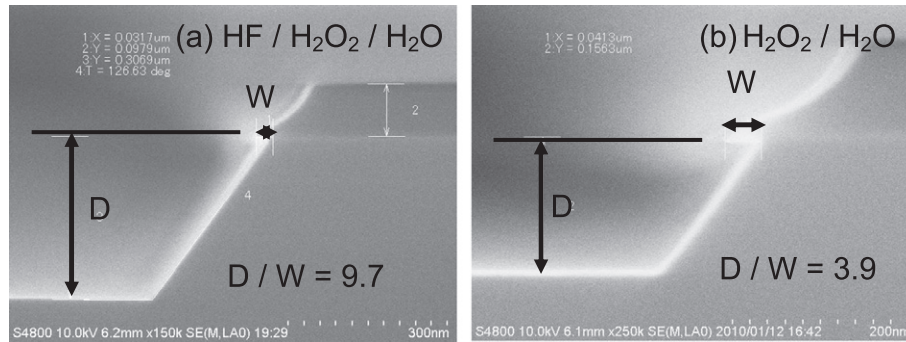


Fig. 2. SEM images of recessed Ge anisotropically etched with (a) HF + H₂O₂ solution and (b) H₂O₂ solution.

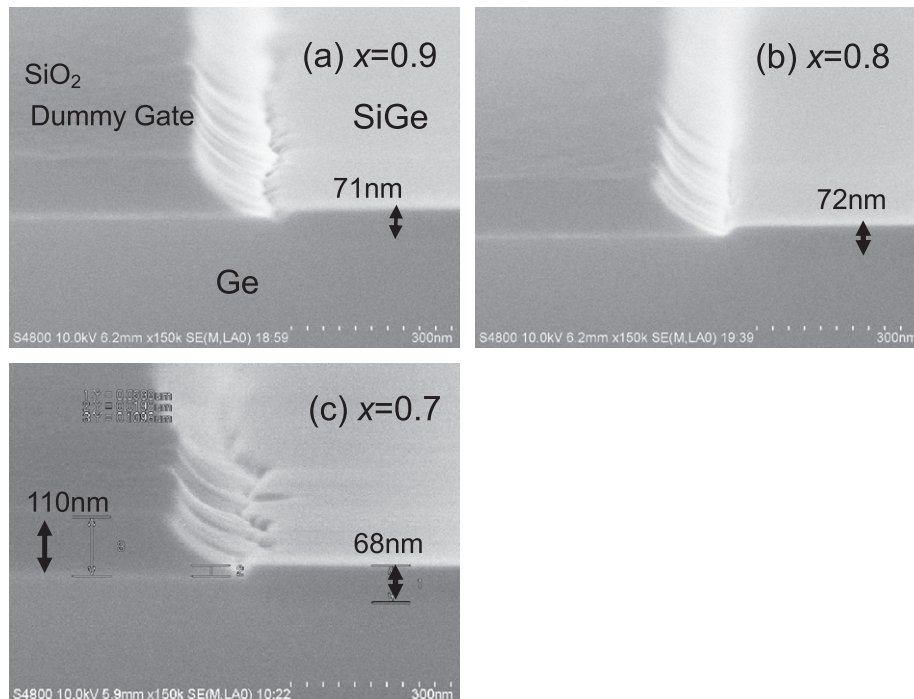


Fig. 3. SEM images of the embedded SiGe stressors selectively grown on the recessed Ge region. (a) $x = 0.9$, (b) $x = 0.8$ and (c) $x = 0.7$.

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