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Low-temperature electrical characterization of junctionless transistors

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ABSTRACT

The electrical performance of junctionless transistors (JLTs) with planar structures was investigated under low-temperature and compared to that of the traditional inversion-mode (IM) transistors. The low-field mobility (μ_0) of JLT devices was found to be limited by phonon and neutral defects scattering mechanisms for long gate lengths, whereas scattering by charged and neutral defects mostly dominated for short gate lengths, likely due to the defects induced by the source/drain (S/D) implantation added in the process. Moreover, the temperature dependence of flat-band voltage (V_{fb}), threshold voltage (V_{th}) and subthreshold swing (S) of JLT devices was also discussed.

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1. Introduction

Junctionless transistors (JLTs) are currently in the spotlight, owing to the advantages which are expected from their simple structure, without PN junctions, and from their operation principle, based on bulk conduction instead of surface conduction for the standard inversion-mode (IM) MOSFET [1]. For example, JLT devices are known as more robust than IM transistors in terms of effective gate length variability and mobility degradation by transverse electric field. However, JLT devices are facing some issues such as mobility degradation by their high channel doping, reduced gate controllability due to partial depletion regions, and threshold voltage variability induced by fluctuation of silicon thickness and doping atoms spatial distribution. Many specific electrical properties of JLT devices have been investigated, so far mainly at room temperature [1–4]. In particular, JLT devices with planar structures recently revealed very interesting features, including two peaks in the plots of transconductance derivative, which distinguish the (bulk) neutral and (surface) accumulation channels [5]. Only few papers have dealt with low temperature operation, concentrating mainly on the identification of conductance oscillations in nanowire JLTs [6], and on temperature dependence of the threshold voltage of such narrow structures [7]. More generally, low-temperature characterization allows for a better understanding of physical operation and electrical performance of electronic devices [8,9]. Extraction of the electrical parameters of JLT devices in the low-temperature range is a powerful tool to get deeper insight into their operation mechanism and more quantitative information about their performance.

This paper deals with JLT devices with a planar structure (W = 10 μm) fabricated from silicon on insulator (SOI) wafers with a silicon thickness t_{si} of 9.4 nm. The electrical parameters of JLT devices were extracted at low-temperature and compared to those of IM transistors fabricated by the same process including an additional implantation on source and drain (S/D) regions, except for channel doping concentration. The electrical performances of JLT devices, including scattering mechanisms and short channel effects, are discussed based on an analysis of temperature dependence of low-field mobility, threshold voltage, flat-band voltage and subthreshold swing.

2. Device fabrication and experiment

This study was based on N-type JLT devices with high-κ/metal gate stack, fabricated at CEA-LETI on (100) SOI wafers with

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145 nm thick buried oxide (BOX) and a Si body thinned down to 9.4 nm. A full-sheet implantation was performed before active patterning with a phosphorus doping targeted at $1 \times 10^{19}\ \text{cm}^{-3}$ or $2 \times 10^{19}\ \text{cm}^{-3}$. The gate is composed of HfSiON/TiN/Polysilicon, with an equivalent oxide thickness of 1.2 nm. An additional implantation was performed to S/D regions with the aim of improving electrical performance by reducing access resistance. The S/D implantation process (doping level $\approx 10^{20}\ \text{cm}^{-3}$) is exactly same with that of IM transistors. Fig. 1 displays the schematic architecture of the fabricated JLT devices, as well as a transmission electron microscopy (TEM) cross-section showing well defined gate stack on the thinned Si channel. On-mask gate length L_M ranged from 1 μm down to 30 nm and on-mask gate width W_M was 10 μm.

The I–V current–voltage characteristics were recorded using an HP4156b measurement unit, while temperature was varied from 80 K to 350 K. The channel length difference ΔL between effective and on mask channel lengths, which amounted to 10 nm, was obtained by the transfer length method (TLM) [10].

3. Experimental results and discussion

3.1. I–V characteristics at low-temperature

Drain current (I_d) of JLT devices for short and long gate lengths (i.e. effective length L_{eff} = 20 nm, and L = 1 μm, respectively) was measured as a function of gate voltage (V_g), with temperature varying in the range of 80–350 K (Fig. 2a and c). The common intersection point, the so called zero-temperature coefficient (ZTC) point [11], where I_d does not depend on temperature due to the compensated temperature effects of mobility and conduction threshold voltage (V_{th}), was found only for long gate lengths (Fig. 2c). This feature is explained from the fact that V_{th} and carrier mobility were both increased at decreasing temperature for long gate length, while they varied in opposite directions (increased and decreased, respectively) at decreasing temperature for short gate length. In contrast, for IM transistors featuring the same structure as JLT devices (Fig. 3a and c), the ZTC was found for both short and long gate lengths, consistently with an increase of V_{th} and carrier mobility at low temperature, whatever the gate length.

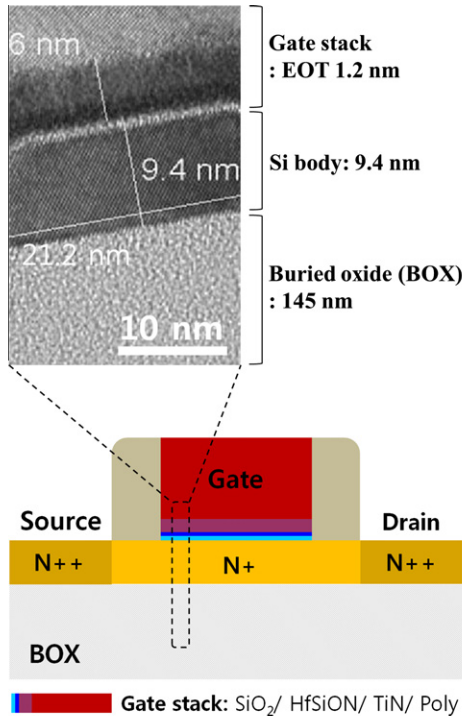

Fig. 1. Schematic architecture of the fabricated JLT devices (lower) and transmission electron microscopy (TEM) cross-section showing well defined gate stack with thinned Si body (upper). An HfSiON/TiN/Polysilicon gate stack (EOT = 1.2 nm) was used and an additional source/drain (S/D) implantation was performed to reduce S/D access resistance.

For JLT devices, the corresponding transconductance (g_m) and transconductance derivative (dg_m/dV_g) were plotted in Fig. 2b and d, respectively. Two peaks were observed on the dg_m/dV_g plots (red[1] curve), but for long gate length only (Fig. 2d), owing to reduced mobility degradation and series resistance effects as compared to short gate length. The existence of these two peaks in long JLTs is a clear difference with IM transistors [5], which normally show one single peak regardless of gate length as confirmed in Fig. 3b and d. As already discussed in a previous paper [5], the first peak (left-hand side peak) in Fig. 2d is representative of V_{th}, which corresponds to the turning point from full to partial depletion in the channel, whereas the second peak (right-hand side peak) gives the flat-band (V_{fb}) position, separating bulk neutral channel from surface accumulation. Interestingly, dg_m/dV_g plots in Fig. 2d clearly show that the V_{fb} and V_{th} of JLT devices were increased at decreasing temperature. The V_{th} of IM transistors, derived from the peak points in dg_m/dV_g plots as shown in Fig. 3b and d, was also increased at low temperature.

3.2. Temperature dependences of threshold and flat-band voltage

The temperature dependence of V_{fb} and V_{th} is displayed in Fig. 4a for JLT devices with a long gate (L = 1 μm). The positions of the first and second peaks in the dg_m/dV_g plots (Fig. 2d) were selected for the determination of V_{th} and V_{fb}, respectively. It is known that the V_{th} of JLT devices can be derived from the depletion approximation or the charge-based analytical model according to the following equation, valid for wide structures [3,12]:

$$V_{th} = V_{fb} - \frac{q \cdot N_d \cdot t_{si}^2}{2\varepsilon_{si}} - \frac{q \cdot N_d \cdot t_{si}}{C_{ox}} \tag{1}$$

where q, N_d, ε_{si} and C_{ox} denote electronic charge, doping concentration in the channel, silicon permittivity and gate oxide capacitance per unit area, respectively. From Eq. (1), threshold voltage variation with temperature (dV_{th}/dT) should be equal to the flat-band voltage variation (dV_{fb}/dT), because the V_{th} term in Eq. (1) contains temperature independent parameters only, except for V_{fb}. This explains why there was no significant difference between the variations of V_{th} and V_{fb} with temperature in Fig. 4a. In addition, the V_{fb} and dV_{fb}/dT of JLT devices can be written as an explicit function of temperature, as:

$$V_{fb} = \Phi_{MS} = \Phi_M - \left[\chi + \frac{E_g}{2} - \frac{k \cdot T}{q} \cdot \ln\left(\frac{N_d}{n_i}\right)\right] \tag{2}$$

$$\frac{dV_{fb}}{dT} = \frac{dV_{th}}{dT} = \frac{k}{q} \cdot \ln\left(\frac{N_d}{n_i}\right) - \frac{k \cdot T}{q} \cdot \frac{1}{n_i} \cdot \frac{dn_i}{dT} \tag{3}$$

where Φ_M, χ, k and n_i denote metal work function, electron affinity, Boltzmann constant and intrinsic carrier density, respectively. The n_i is also affected by temperature according to following relationship [13]:

$$n_i \approx n_{i0} \cdot T^{\frac{3}{2}} \cdot e^{-\frac{E_g}{2kT}} \tag{4}$$

where E_g is the energy band-gap and n_{i0} is around $3.9 \times 10^{16}\ \text{cm}^{-3}$ in silicon. The dV_{fb}/dT value of ≈ -0.56 mV/K which was extracted

[1] For interpretation of color in Fig. 2, the reader is referred to the web version of this article.

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