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An analytical threshold voltage model for graded channel asymmetric gate stack (GCASYMGAS) surrounding gate MOSFET

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Abstract

A new structural concept, graded channel asymmetric gate stack (GCASYMGAS) SGT has been proposed and a two-dimensional analytical model is developed to examine the impact of this structure in suppressing short channel effects and in enhancing the device performance. It is shown that incorporation of ASYMGAS and graded channel designs leads to improved short channel immunity and hot carrier reliability. It is also demonstrated that for GCASYMGAS the average electric field in the channel is enhanced which leads to an increase in the electron velocity thereby improving the carrier transport efficiency. Furthermore, the device characteristics have been studied over a wide range of parameters and bias conditions and it is found that GCASYMGAS offers superior characteristics as compared to UD and GC devices. The results so obtained have been compared with simulated data obtained from the device simulator ATLAS 3D and are found to be in good agreement.

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1. Introduction

Steady downscaling of device dimensions, innovative device designs and rapid advances in technology are some of the factors that have largely governed the evolution of CMOS technology at a remarkable rate over the last few decades. As a result denser and faster integrated circuits have been achieved that offer superior performance and much reduced physical size compared to their predecessors. However, the continued miniaturization of the classical bulk MOSFET leads to short channel effects and a reduction in current drivability. These are major reliability issues and assume concern as they present a serious challenge to the key objective of further downscaling while maintaining a high device performance. In order to overcome the scaling limitations and to enhance the device performance various nonclassical structures such as Pi gate MOSFETs, Omega MOSFET, Cylindrical/Surrounding gate MOSFETs have been proposed. Among these, the surrounding gate MOSFET [1–6], in particular, has drawn a great deal of attention as it offers high packing density, steep subthreshold characteristics and higher current drive. Another remarkable feature of this structure is that the gate surrounds the silicon pillar completely and therefore controls the channel potential in a more effective manner resulting in increased short channel immunity. All these features make the SGT a potential candidate to succeed the classical planar MOSFET.

Recently various channel engineered structures have also been proposed in an attempt to address the issues of

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short channel effects and hot carrier degradation which degrade the device characteristics and impose a limit on device scaling [7–13]. The graded channel (GC) design in which the doping is kept high near the source side and low near the drain end has been paid great deal of attention as it provides excellent immunity against the short channel effects and also improves the hot carrier reliability of the device as it leads to a reduction in hot carrier effects and impact ionization. Besides these advantages the GC design also leads to a higher drive current and enhancement in transconductance as compared to the uniformly doped devices [11,12].

The downsizing of CMOS technology in the nanoscale regime has also necessitated the requirement for ultra-thin gate dielectrics with thicknesses less than 3 nm. However, the extent to which the gate oxide thickness can be scaled down is limited by direct tunneling which can lead to an increase in the gate leakage current thus degrading the device reliability. It also leads to an increase in static power consumption which can affect the circuit operation [14]. In order to overcome this limitation, emphasis has been laid on the use of high-k dielectrics as alternative gate insulator materials to prevent direct tunneling leakage current. However, the studies have demonstrated that replacing SiO_2 with high-k gate dielectrics degrades the device performance due to increased fringing fields from the gate to the S/D regions which weakens the control of gate over the channel. The high-k/Si system also results in unacceptable level of bulk fixed charge, high interface trap density and low silicon interface carrier mobility [14]. Therefore, an extremely thin layer of interfacial oxide is used as a passivating layer to minimize interface trap density and it has been shown that a dielectric stack structure improves the device performance [15]. The asymmetric gate stack structure (ASYMGAS) was proposed in order to reduce the gate leakage and it has been shown that it also leads to an enhancement in the average electric field in the channel thereby, improving the carrier transport efficiency [16,17].

In order to incorporate the advantages of both the GC and ASYMGAS structures, a novel device architecture graded channel asymmetric gate stack (GCASYMGAS) is proposed and a two-dimensional analytical model is presented to examine the impact of this structure on device characteristics. It has been demonstrated that GCASYMGAS enhances the short channel immunity and hot carrier reliability while also resulting in increased gate controllability and improved transport efficiency as compared to GC and UD devices. In order to gain an insight into the effectiveness of GCASYMGAS design, the device characteristics have been compared over a wide range of parameters and bias conditions and it is shown that GCASYMGAS structure achieves the twin objective of miniaturization and high device performance. The accuracy of the model was verified by comparing the analytical results with simulated data obtained using 3D device simulator ATLAS.

2. Model formulation

The schematic diagram of a graded channel asymmetric gate stack cylindrical/surrounding gate (GCASYMGAS) MOSFET is shown in Fig. 1. As can be seen, the doping in the channel is kept high in a region L_1 near the source side and low in a region L_2 near the drain side such that the total channel length L, $L = L_1 + L_2$. Also as can be seen there is a single gate oxide (SGO) region near the source and a gate stack oxide (GSO) region near the drain. The analysis has been done assuming that there is no lateral diffusion of doping across the interface [18,19]. Furthermore, the model does not account for quantum effects since the channel length and silicon film thickness considered in the analysis are greater than 30 nm and 10 nm respectively [20,21].

Assuming the impurity density in the channel to be uniform and neglecting the influence of charge carriers, the Poisson equation in cylindrical coordinates for the two regions can be written as:

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial \phi_k(r,z)}{\partial r}\right)+\frac{\partial^2 \phi_k(r,z)}{\partial z^2}=\frac{qN_{ak}}{\varepsilon_{si}} \tag{1}$$

where, $\phi_k(r,z)$ is the potential distribution in the silicon film, N_{ak} is the doping concentration with $k=1$ for region 1 near the source and $k=2$ for region 2 near the drain end.

The potential distribution in the silicon film in the two regions is assumed to be a parabolic profile in the radial direction [22] and can be written as:

$$\phi_1(r,z) = p_{01}(z) + p_{11}(z)r + p_{21}(z)r^2, \quad 0 \leqslant z \leqslant L_1 \tag{2}$$

$$\phi_2(r,z) = p_{02}(z) + p_{12}(z)r + p_{22}(z)r^2, \quad L_1 \leqslant z \leqslant L_1 + L_2 \tag{3}$$

where, the coefficients p_{0k}, p_{1k} and p_{2k} are the functions of z.

The Poisson equation in the two regions is solved separately using the boundary conditions [23,24] to obtain the surface potential in the high and low doped regions as:

$$\phi_{s1}(z) = C_{11}\exp\left(\frac{-z}{\lambda_1}\right)+C_{12}\exp\left(\frac{z}{\lambda_1}\right)-\omega_1 \tag{4}$$

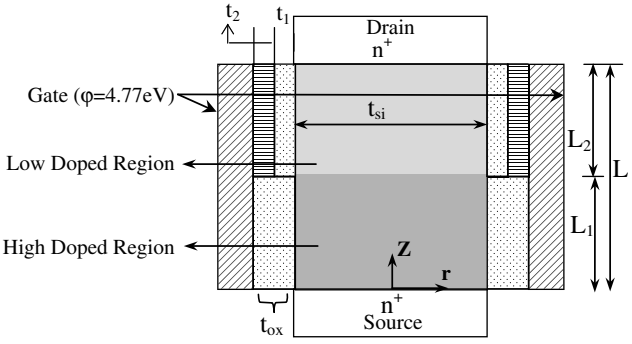

Fig. 1. Cross-sectional view of a GCASYMGAS SGT.