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Letter

Investigation of gate length and fringing field effects for program and erase efficiency in gate-all-around SONOS memory cells

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ABSTRACT

Gate length (L_G) effects for program/erase (P/E) efficiency are investigated in a gate-all-around (GAA) SONOS structure. The experimental results show that P/E characteristics become worse at a shorter L_G, and this trend is verified with numerical simulation. The down-scaling of L_G gives rise to a change in the electric field in tunneling oxide and blocking oxide in the GAA–SONOS structure. For P/E efficiency, these results reveal that the fringing field via a low-*k* dielectric medium, which encapsulates a gate electrode as an inter-layer dielectric, favorably enhances the electric field of tunneling oxide. It also reduces the electric field of blocking oxide. Additionally, it is found that the electric field of tunneling and blocking oxide becomes more sensitive to the permittivity of the inter-layer dielectric as L_G is more shortened.

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1. Introduction

Recently, nonvolatile memory (NVM) devices, which can sustain data without continuous electric power supply, are widely used for mobile applications. Although the technology of floating-gate devices has been remarkably developed to make high density devices, it faces critical scaling limits, cell-to-cell interference [1,2]. On the other hand, silicon-oxide–nitride-oxide–silicon (SONOS) devices are regarded as being noteworthy because they have better immunity against cell-to-cell interference [3]. Meanwhile, a gate-all-around (GAA) field-effect-transistor (FET) showed the highest robustness against short-channel effects (SCEs) [4,5] compared to single-gate, double-gate [6], triple-gate [7], and omega gate [8]. In the case of GAA SONOS-type devices, the electric field of tunneling oxide is much higher than that of blocking oxide by virtue of the cylindrical geometry [9]; hence, the program/erase (P/E) efficiency of the GAA structure was superior to that of the aforementioned structures. Therefore, the GAA–SONOS structure can be a promising candidate for 3-dimensional (3-D) geometric NAND flash memory and 3-D multi-stacking devices [10].

It was previously reported that the P/E efficiency degraded as L_G was scaled down in a conventional 2-dimensional (2-D) SONOS structure [11]. Although the GAA–SONOS structure has demonstrated excellent performances, consideration of P/E efficiency with respect to the down-scaling of L_G has not yet been investigated comprehensively [9,12]. Thus, it is the right time to study how gate length scaling influences P/E efficiency in the GAA–SONOS structure.

In this work, the GAA–SONOS structure is fabricated, and its P/E efficiency is investigated for various L_G's. From the numerical simulations, the electric field in the oxide/nitride/oxide (O/N/O) stack of the GAA–SONOS structure is analyzed from the point of view of P/E. Moreover, the electric field dependency on the permittivity of the inter-layer dielectric, which encapsulates the gate electrode, is investigated.

2. Device fabrication

The process flow of GAA–SONOS devices is the same as in our previous work except for the formation of O/N/O stacks [13]. O/N/O layers with a thickness of 3 nm/6 nm/8 nm were made of the thermally grown oxide, the nitride deposited by low-pressure chemical vapor deposition (LPCVD), and the deposited oxide (tetraethyl orthosilicate: TEOS) by LPCVD, respectively. The S/D was doped with arsenic at a dose of $5 \times 10^{15}/cm^2$ and the dopant was activated by a rapid thermal annealing (RTP) process at 1000 °C

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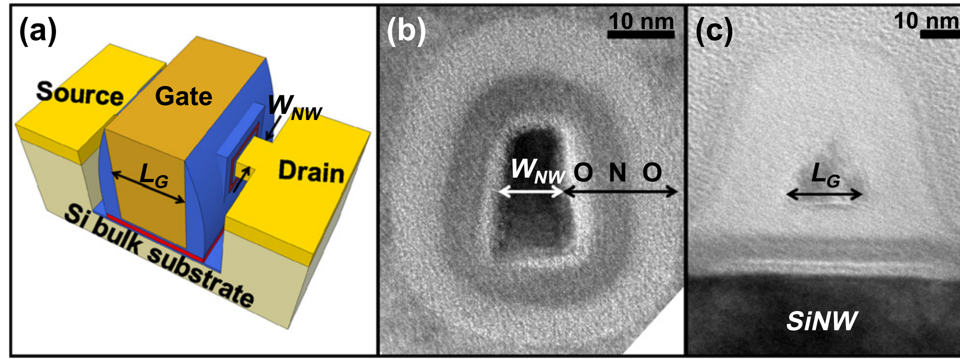

Fig. 1. Schematic and cross-sectional TEM images. (a) Schematic of the GAA–SONOS device on the bulk substrate. (b) A cross-sectional TEM image of the fabricated silicon nanowire in the GAA–SONOS device. W_{NW} is 10 nm and the thicknesses of the O/N/O stack are 3/6/8 nm, respectively. (c) A TEM image along the channel length direction. L_G is 20 nm.

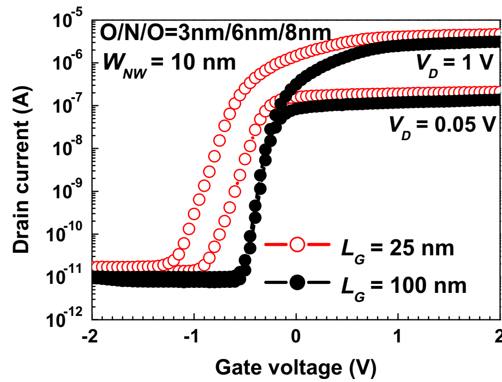

Fig. 2. Characteristics of I_D versus V_G at V_D values of 0.05 and 1 V for the GAA–SONOS memory cells with the O/N/O gate dielectric. W_{NW} is 10 nm and the thicknesses of the O/N/O stack are 3/6/8 nm, respectively.

for 3 s. Numerical simulations were carried out using ATLAS of SILVACO [14]. Fig. 1b shows the cross-sectional transmission electron microscopy (TEM) image of the GAA–SONOS structure. The width of the silicon nanowire (W_{NW}) is 10 nm. Fig. 1c shows a TEM image of L_G direction. L_G of the image is 20 nm. Fig. 2 shows the typical transfer characteristics of the fabricated GAA–SONOS cells for different L_G values.

3. Device characteristics and discussion

3.1. Programming efficiency

Pulsing signals are applied to the gate while keeping the source/drain grounded during program and erase operations. The threshold voltage (V_T) is defined as the gate voltage when the drain current reaches 100 W/L nA. Fig. 3a shows the measured typical program characteristics of GAA–SONOS memory cells. A shift of V_T gradually decreases as L_G shortens under the same programming condition. This is because the maximum electric field of the tunneling oxide is lowered as L_G is reduced, as simulated in Fig. 4a. The lowered electric field in the tunneling oxide can be understood by the augmented fraction of fringing field for a shortened L_G device. When the fringing field is intentionally eliminated in the simulation, we observed that the actual electric field of the tunneling oxide is not changed for various L_G devices (data are not shown). Thus it is inferred that the control of fringing field plays a critical role in managing the programming efficiency.

3.2. Erasing efficiency

Fig. 3b shows typical erase characteristics of the GAA–SONOS memory cells. Before the erase operations, the selected devices were programmed by a different pulse time to adjust the programmed V_T to be 4 V. The erasing saturation, which is considered as one of the concerns in a SONOS-type device, is the phenomenon

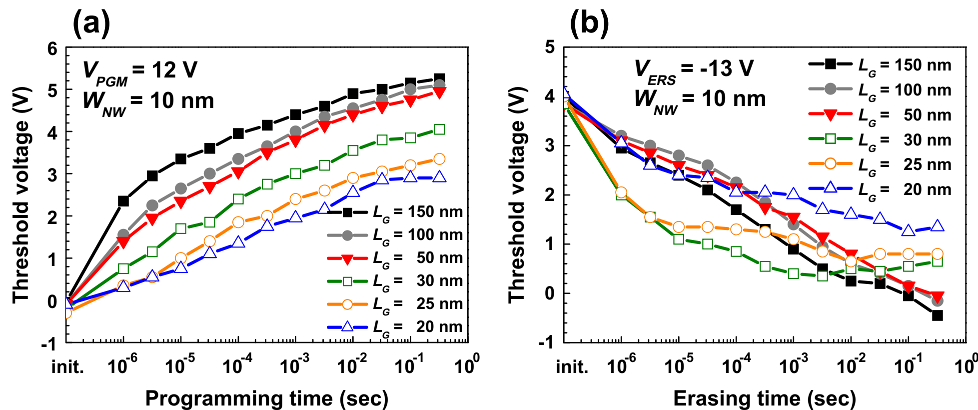

Fig. 3. Measured program and erase efficiency. (a) programming and (b) erasing characteristics of the GAA–SONOS memory cells. A range of L_G is from 20 nm to 150 nm. Appropriate pulse times are applied to the gate and adjusted to produce 4 V of initial V_T while keeping the source/drain grounded.

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