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$Ge_2Sb_2Te_5$ layer used as solid electrolyte in conductive-bridge memory devices fabricated on flexible substrate

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ABSTRACT

This paper shows that the well-know chalcogenide $Ge_2Sb_2Te_5$ (GST) in its amorphous state may be advantageously used as solid electrolyte material to fabricate Conductive-Bridge Random Access Memory (CBRAM) devices. GST layer was sputtered on preliminary inkjet-printed silver lines acting as active electrode on either silicon or plastic substrates. Whatever the substrate, the resistance switching is unambiguously attested at a nanoscale by means of conductive-atomic force microscopy (C-AFM) using a Pt–Ir coated tip on the GST surface acting as a passive electrode. The resistance change is correlated to the appearance or disappearance of concomitant hillocks and current spots at the surface of the GST layer. This feature is attributed to the formation/dissolution of a silver-rich protrusion beneath the AFM tip during set/reset operation. Beside, this paper constitutes a step toward the elaboration of crossbar memory arrays on flexible substrates since CBRAM operations were demonstrated on W/GST/Ag crossbar memory cells obtained from an heterogeneous fabrication process combining physical deposition and inkjet-printing.

1. Introduction

Resistive Random Access Memories (RRAM) are attracting intensive and increasing research efforts as potential high-density information storage solutions beyond the 15 nm node [1–3]. Various physical phenomena are known to lead to a non-volatile resistive switching effect which are related to different types of RRAM such as Thermo Chemical Memories (TCM) or Valency Change Memories (VCM) [4]. The actual driving force for the resistance switching, although electrically induced in all cases, is quite different and depends upon the underlying resistive material. Among the main types of RRAM devices, Electro-Chemical Metallization memory cells (ECM), also referred as Conductive-Bridge Random Access Memories (CBRAM) or Programmable Metallization Cells (PMC) [5], are of particular interest due to their low-voltage operations [6,7], their large retention capabilities for more than 10-years [7] and their endurance larger than 10^5 cycles [8,9]. The memory elements simply rely on a solid electrolyte sandwiched between an electrochemically active metallic electrode (*i.e.* Cu or Ag) and an inert counter-electrode (such as Pt or W). The memory effect is achieved through redox mechanisms enabling the electro-migration of dissolved positives ions (*e.g.* Ag^+ or Cu^+) leading to an electro-deposition (set operation) or dissolution (reset operation) of metallic filaments between the two electrodes. Most of the solid electrolyte materials consist in a chalcogenide glass such as GeSe [7], GeS [10], Cu_2S [11] or oxide glasses such as SiO_2 [12] or Ta_2O_5 [13]. An extensive summary of the electrolyte/electrode couples employed in CBRAM devices can be found in the recent work published by Valov et al. [5]. Although some works recommended the use of $Ge_2Sb_2Te_5$ (GST) layers as a way to improve the electrical behavior of CBRAM devices in terms of power consumption [14], resistance ratio (R_{OFF}/R_{ON}) [15] or electrical variability [16], few reports mention its use as a solid electrolyte. In previous works Pandian et al. [17–19] showed that crystallized Sb-rich GST layers exhibit Polarity Dependent Resistance (PDR) switching which was attributed to the formation/dissolution of Sb conductive filaments bridging together $Ge_2Sb_2Te_5$ crystalline grains and both electrodes through the amorphous GST phase. In complement to previously published works, the

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present paper demonstrates that amorphous $Ge_2Sb_2Te_5$ layer can also be used as a solid electrolyte in CBRAM devices employing silver as the active electrode. Using an heterogeneous fabrication process combining printed and/or sputtered electrodes and sputtered GST layer, CBRAM memory effect is clearly evidenced in the GST layer either at a nanoscale by conductive atomic force microscopy (C-AFM) or at a micrometric scale on crossbar cells with a W top electrode. In addition, in a context of constant development of new applications lying beside the silicon solid-state devices, memory material stacks were deposited on a flexible plastic substrate in view of future low-voltage embedded applications such as RFID (Radiofrequency Identification) systems.

2. Experimental details

Fig. 1 illustrates the main fabrication steps of the samples. The substrates consisted in either Si (100) wafers covered by a 200 nm-thick SiO_2 layer or 120 μm-thick polyimide (Kapton® 500-HN) foils. At first, silver lines (350 nm-thick, 100 μm wide) were deposited by inkjet printing of a commercial silver ink (Sun-Chemical EDM5603) consisting of Ag nanoparticles with a diameter of about 80 nm in a mixture mainly composed of ethanediol and ethanol. The used printing head is a Spectra Galaxy JA 256/30 AA, providing ink drops of 30 pL. A printing resolution of 608 dpi was used. The patterns were printed at 300 mm/s (Fig. 1a). The samples were then annealed during 30 min at 200 °C in order to eliminate the organic solvent and favor the coalescence of the silver nanoparticles to produce conductive lines. The resulting silver lines were then covered by a GST thin film (thickness varying from 20 to 150 nm) deposited by radiofrequency (RF) magnetron sputtering from a high-purity (99.9999%) stoichiometric $Ge_2Sb_2Te_5$ target through a shadow mask (Fig. 1b). Some of the samples were finally covered by an inert counter top electrode, consisting of W lines (200 nm thick, 100 μm wide) deposited by RF-magnetron sputtering through a shadow mask perpendicularly to silver lines to produce crossbar devices (Fig. 1c). The amorphous state of the GST layer after deposition on SiO_2/Si substrates was attested by means of X-ray diffraction [20].

Fig. 2a shows a picture of a sample taken after the GST deposition (fabrication stage of Fig. 1b). The sample was also characterized by scanning electron microscope (SEM) at the same fabrication stage. The SEM cross-section of Fig. 2b shows a 135 nm-thick GST layer deposited on Ag printed lines on a Kapton® foil. The micrograph clearly shows a rough interface between the silver lines and the GST layer due to an incomplete coalescence of the Ag nano-particles during post-printing annealing.

The resistance switching in the memory stack (*i.e.* GST/Ag) was deeply investigated at nanoscales by means of conductive atomic force microscopy (C-AFM) on samples without a top electrode. The measurements were conducted on a Veeco Dimension 3100 with a Nanoscope V controller and platinum–iridium (Pt–Ir) conductive tip enabling the measurement of the local electrical conductivity. Local current–voltage characteristics were measured by applying a voltage bias to the bottom electrode, the AFM tip being grounded. Fig. 3a shows a 5 μm × 5 μm atomic force microscope (AFM) image obtained in contact mode on a 35 nm-thick GST layer using an insulating silicon nitride tip. The calculated root mean square roughness of this topography map was 14.2 nm which is very close to the one obtained directly on the silver bottom electrode (14.6 nm). This result, in conjunction to the very low roughness measured on the same GST layer deposited on SiO_2/Si substrates [20], suggests that the roughness of the GST layer originates from the underlying printed silver electrode. This was confirmed by the extraction of cross-section profiles obtained either on the GST layer (Fig. 3b) or on the silver electrode (Fig. 3c) which exhibited similar roughness profiles.

3. Results and discussion

3.1. Resistive switching at a nanoscale on GST/Ag/SiO_2/Si stack

Atomic Force Microscopy (AFM) and its derivative electrical techniques have demonstrated their usefulness in studying resistive switching effects at a nanoscale [21–23]. Using a conductive Pt–Ir coated tip, current spectroscopy measurements were performed by means of C-AFM on a 35 nm-thick GST layer deposited on Ag printed lines. In those experimental conditions, the conductive AFM tip acts as a top electrode. While applying voltage sweeps in a range between −1.0 V and +1.0 V to the bottom electrode, the conductive tip being grounded, a neat hysteresis cycle loop is observed on the current–voltage characteristics as shown in Fig. 4 where the different steps of the switching process are marked from 1 to 6. More precisely, at a bias voltage of 0.25 V the current level flowing through the tip suddenly overpasses the saturation current of the C-AFM sensor (*i.e.* 1.2 μA) (loop parts 1 → 3), the sample reaching a low resistance state (LRS). During the reverse sweep the *I–V* characteristic exhibits an ohmic behavior (4 → 5) down to a voltage of −0.1 V. Below this voltage, an abrupt current drop is observed, the measured current going down to the detection limit of the sensor (5 → 6) indicating that the sample returned back to a high resistance state (HRS).

This hysteretic *I–V* characteristic was measured while positioning randomly the tip on the GST layer and was observed in a very reproducible way at different locations on the sample; holding the tip at a fixed position, more than 10 switching cycles could be repeatedly obtained at a scan rate of 1 Hz without observing any thermal drift effects (*i.e.* tip sliding out of the probed region). The

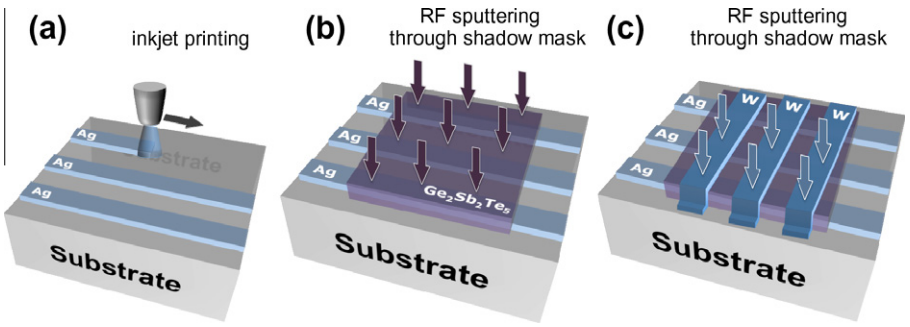

Fig. 1. Description of the main fabrication steps of the studied devices. (a) Silver electrodes were obtained from printing of silver ink on substrates consisting either in SiO_2 (200 nm)/Si wafers or plastic foils. (b) A GST layer was then deposited by radiofrequency magnetron sputtering on top of the silver lines through a shadow mask. (c) Finally W lines were sputtered through a shadow mask to form crossbar memory structures.