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The fabrication and the reliability of poly-Si MOSFETs using ultra-thin high-*K*/metal-gate stack

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ABSTRACT

Poly-Si MOSFETs using a gate stack composed of ultra-thin $HfSiO_x$ and TiN are shown, and they are compatible with a monolithic three-dimensional integrated circuit (3D-ICs) process with the highest thermal budget of 700 °C. The poly-Si MOSFETs were studied for fabrication process temperatures with parasitic resistance, effective gate length, and grain boundary trap density. The short-channel effect with V_T (threshold voltage), subthreshold swing (SS), and drain-induced barrier lowering (DIBL) was also compared at 650 °C and 700 °C. For stress reliability of both hot carrier and PBTI, the short-channel devices showed more stability in V_T than the long-channel devices due to less grain boundary scattering. This study promotes the ultra-thin high-*K*/metal gate poly-Si MOSFET as a candidate for future monolithic 3D-ICs and silicon-on-glass (SOG) applications.

1. Introduction

The 3D-ICs (three-dimensional integrated circuits) are believed to be one of the candidates for IC structures beyond Moore's law as scaling down to reach physical limit in the future. Furthermore, the sequential fabrication process [1] of monolithic 3D-ICs has a cost advantage when compared to wafer-bonding processes [2]. Recently, poly-Ge with high mobility had been reported for monolithic 3D ICs [3], whose relatively bad on/off ratio due to high transistor leakage becomes an issue for development. For the high-performance upper transistors to be compatible with CMOSFETs, a base layer is needed. The high-*K*/metal gate (HK/MG) poly-Si (polycrystalline silicon) MOSFETs could be a solution, which is operated by a high driving current and a steep swing, due to the low thermal budget involved in their fabrication [4], as shown in Fig. 1a. In the flat panel display industry, the poly-Si TFTs have a low-temperature process to meet the requirements of monolithic 3D-ICs, which are processed after base transistors. The hafnium-based oxide becomes a necessity to develop high-*K* gate-dielectric material in MOSFETs due to its high-*K* value (~25), wide bandgap, acceptable band alignment, and superior thermal stability [5]. Poly-Si TFTs with thick hafnium-based oxide (>20 nm) have been reported, and the subthreshold swing (SS) as 280 mV/dec [6] and 300 mV/dec [7] for n- and p-channels, respectively. This work discusses the fabrication and the reliability of the integrated ultra-thin $HfSiO_x$ and TiN gate stack with poly-Si for high-performance applications, such as monolithic 3D-ICs and system on glass (SOG).

2. Device fabrication

High-performance poly-Si TFTs were fabricated with a design rule of 0.3 μm in a 150-mm wafer line. The fabrication was started by depositing an amorphous Si (α-Si) layer at 550 °C by Low Pressure Chemical Vapor Deposition (LPCVD) on Si wafers capped with a 0.6-μm thick oxide layer. The deposited α-Si layer was then recrystallized by a solid-phase crystallization (SPC) process at 600 °C in a N_2 ambient. The observed grain size and the roughness of the 300-nm poly-Si with SPC crystallization were 100–150 nm (SEM) and roughly 3 nm (AFM), respectively; the surface morphology is shown in Fig. 2a. The average grain size in this material was larger than that of a conventional TFT process for the 50-nm-thick poly-Si, as shown in Fig. 2b, but their roughness was relatively similar. The grain size conformed with the prior results [8], and typically was 20–45 nm for 50-nm-thick poly-Si. Then, after removing the native oxide by dipping it in a diluted HF solution, an ultra-thin $HfSiO_x$ and a 200-nm TiN were deposited in the combined method of Metal Organic Chemical Vapor Deposition (MOCVD) at 550 °C and sputtering system at room temperature, respectively. The gate stack was defined by lithography and etching process. Next, a self-aligned arsenic ion implantation was performed at 25 keV with a dose of 5×10^{15} cm^{-2} to dope the source/drain region. The annealing process for the dopant activation was performed by RTA in an N_2 ambient with step 1 being at 600 °C for 100 s, and step 2 being at 650 °C, 700 °C, or 730 °C. The bulk

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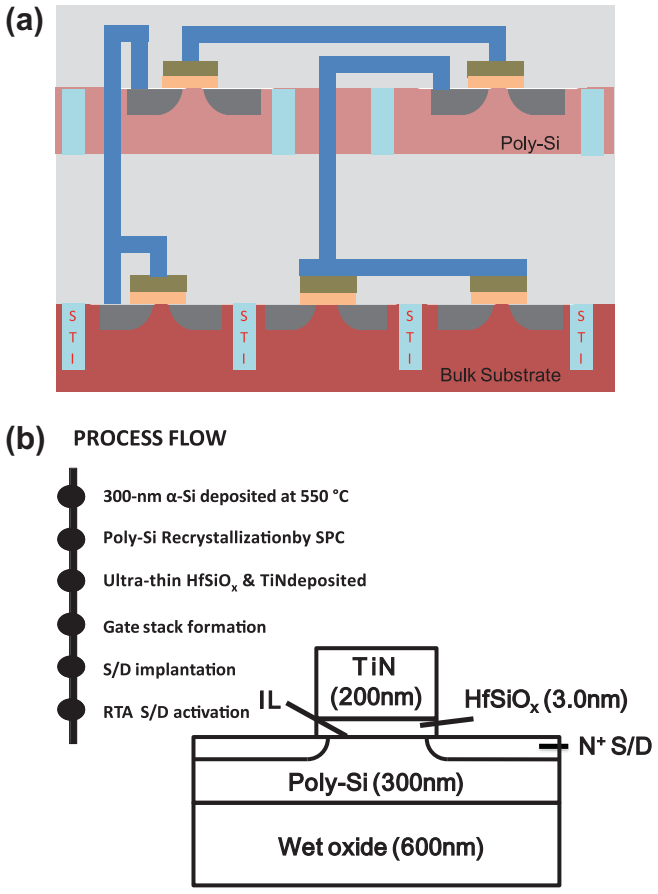

Fig. 1. (a) Schematic diagram of a monolithic 3D-ICs structure. The integrated ultra-thin $HfSiO_x$ and TiN gate stack with poly-Si is used for high-performance upper transistor requirements. (b) The device fabrication process flow and structure. The poly-Si thickness is 300 nm to obtain a larger grain.

Si was also fabricated together with the same process flow for control devices. Fig. 1b shows the device's fabrication process flow and the schematic diagram of the device structure.

3. Results and discussion

Fig. 3 shows the capacitance–voltage characteristics of TiN/$HfSiO_x$ on bulk Si with different annealing temperatures. TiN might react with $HfSiO_x$ to reduce the effective dielectric constant and lower C_{max} for 730 °C Rapid Thermal Annealing (RTA). However, it does not seem enough to form a good-quality interfacial layer and led to higher D_{it} for 650 °C RTA. The capacitance-equivalent thickness (CET) and the effective dielectric constant of $HfSiO_x$ with 700 °C RTA were extracted by bulk Si *C–V* characteristics as 2.8 nm and 9, respectively. Note that the physical thickness of $HfSiO_x$ and the interfacial layer (IL) by HR-TEM were 3.0 and 1.5 nm, respectively, after all the thermal budget of process [9]. Besides, the dopants also diffused into the channel during annealing and made the effective channel length L_{eff} differ from the mask-defined gate length L. The relation was $L_{eff} = L - \Delta L$ and $\Delta L = 2\delta L$ [10], where δL was the dopant diffusion length into the channel from the source or the drain in lateral direction. Fig. 4a shows the series resistance and the ΔL versus gate length with different annealing temperatures. A serious short-channel effect was observed for 730 °C devices due to large ΔL. However, the series resistances improved with a decrease with higher annealing temperatures. There are two possible reasons to explain the drastic increase in the value of ΔL while the annealing temperature is 730 °C. One is the dopant

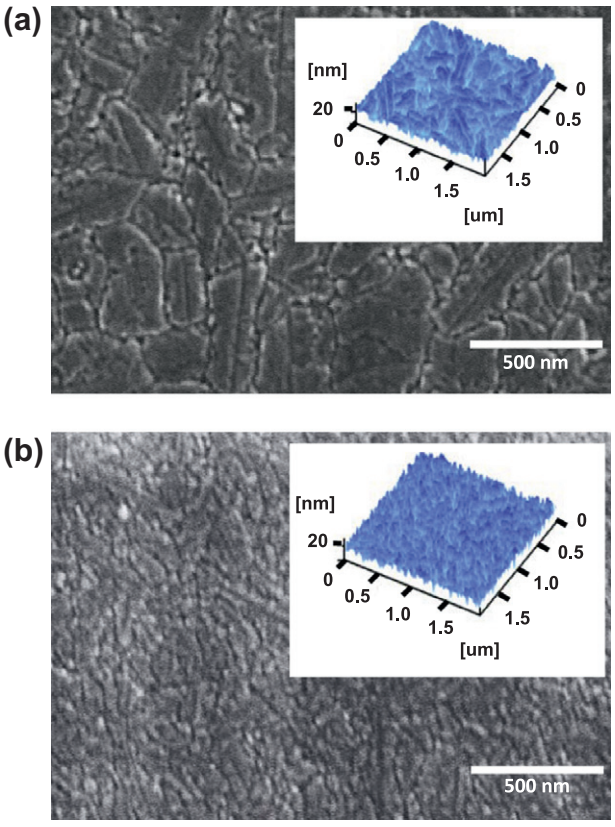

Fig. 2. The SEM image of (a) 300-nm-thick poly-Si and (b) 50-nm-thick poly-Si after SPC 600 °C. The insets show the surface morphologies by AFM. The larger grain size (~150 nm) and similar roughness (~3 nm) of 300-nm poly-Si with SPC recrystallization were obtained in comparison with that of conventional TFT process, which is 50-nm-thick poly-Si.

diffusion series into the channel from a source/drain in lateral direction along the grain boundary. The other one is 730 °C is close to the recrystallization temperature of MOCVD $HfSiO_x$ [11]. The latter indicates the $HfSiO_x$ may partially crystallize and leads to a short-channel effect with increasing gate leakage. The grain boundary trap state density (N_t) was estimated by the Levinson–Proano method [12,13] in Fig. 4b. The N_t was determined from the slopes of these curves. The improvement of N_t was obtained with increasing annealing temperature in Fig. 4b, where 700 °C was chosen as the optimum condition for RTA. The high-*K* $HfSiO_x$

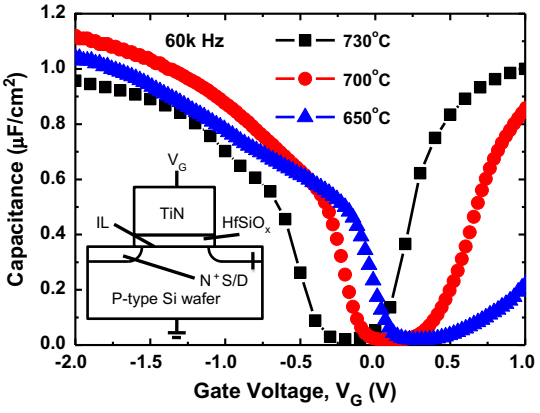

Fig. 3. The *C–V* characteristics of HK/MG on bulk-Si at 60 kHz. The inset shows the schematic diagram of the *C–V* measurement.