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$BaTiO_3$ as charge-trapping layer for nonvolatile memory applications

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ABSTRACT

The charge-trapping (CT) properties of $BaTiO_3$ are investigated by using an $Al/Al_2O_3/BaTiO_3/SiO_2/Si$ structure. The memory device with $BaTiO_3$ as CT layer shows promising performance in terms of large memory window (8.6 V by ±12 V for 1 s), high program speed with low gate voltage (a V_{FB} shift of 2.9 V at +6 V, 100 μs), negligible V_{FB} shift after 10^5-cycle program/erase stressing, and good data retention property (charge loss of 7.9% after 10^4-s 125 °C baking time), mainly due to the high charge-trapping efficiency of the $BaTiO_3$ film, as well as the large barrier height between the $BaTiO_3$ charge-trapping layer and the SiO_2 tunneling layer.

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1. Introduction

Conventional floating-gate nonvolatile memories are approaching their scaling limits mainly due to their difficulties in maintaining high gate coupling ratio and suppressing cross talk between neighboring cells. Metal-Oxide-Nitride-Oxide-Silicon (MONOS) type nonvolatile memories have been considered as a promising candidate to replace the floating-gate counterpart because of their discrete charge-storage and coupling-free properties. Si_3N_4 ($k \sim 7$) was the first dielectric used as charge-trapping layer (CTL). In order to improve the data-storage capability by continual down scaling of the cell size, high-*k* dielectrics have been widely investigated to replace Si_3N_4 as CTL [1–5]. Fig. 1 and Table 1 summarize the band-gap (E_g) and the conduction-band offset with respect to SiO_2 (ΔE_c) of some typical high-*k* dielectrics used as CTL [6]. For a MONOS-type memory device, it tends to have thinner tunneling oxide for higher program/erase (P/E) speeds and lower operating voltages, whereas a thinner tunneling oxide may deteriorate its retention property. Therefore, there is a trade-off between high P/E speeds and good data retention. Among various high-*k* dielectrics, $BaTiO_3$ exhibits some distinguished properties including its large barrier height with respect to SiO_2 (conduction-band offset $\Delta E_c \sim 3.6$ eV) [6] and high dielectric constant ($k \sim 100$ for the perovskite-type structure) [7], both of which are desirable for the charge-trapping layer of nonvolatile memories to improve the P/E speeds and retention properties. However, there have been few reports focusing on $BaTiO_3$ as CTL for charge-trapping-type nonvolatile memory applications [8]. Therefore, we concentrate on the charge-trapping characteristics of $BaTiO_3$ based on MONOS capacitors in this work. Experimental results demonstrated that this memory device with $BaTiO_3$ showed large memory window, high P/E speeds with low operating voltage, as well as good reliability.

2. Experiment

MONOS capacitors with $Al/Al_2O_3/BaTiO_3/SiO_2/Si$ were fabricated on *p*-type silicon wafers. After a standard RCA cleaning, 2-nm SiO_2 was grown on the wafers by thermal dry oxidation. Then 10-nm $BaTiO_3$ was deposited on the SiO_2 by sputtering using a $BaTiO_3$ target in an Ar/O_2 (24 sccm/6 sccm) mixed ambient at a pressure of 3.0 mTorr. Then 15-nm Al_2O_3 as blocking layer was deposited by means of atomic layer deposition using trimethyl–aluminum ($Al(CH_3)_3$) and H_2O as precursors at a substrate temperature of 300 °C. Following that, all the samples went through a post-deposition annealing (PDA) in N_2 ambient at 900 °C for 30 s. Then, Al was evaporated and patterned as gate electrode with a diameter of 100 μm, followed by forming-gas annealing at 300 °C for 20 min. The physical properties of the dielectric films were analyzed by transmission electron microscopy (TEM), X-ray diffraction (XRD) and X-ray photoelectron spectroscopy (XPS). The electrical characteristics of the MONOS capacitors were measured by HP4284A LCR meter and HP4156A semiconductor parameter

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analyzer. Their flat-band voltage (V_{FB}) was extracted from their measured $C–V$ (capacitance–voltage) curve at the capacitance equal to the calculated flat-band capacitance [9].

3. Results and discussion

The inset of Fig. 2a shows the cross-sectional TEM image of the MONOS capacitor with $BaTiO_3$ as CTL, where the thickness of $Al_2O_3/BaTiO_3/SiO_2$ is determined to be 15.6 nm/10.6 nm/2.0 nm respectively. It is also observed that the $BaTiO_3$ film displays an amorphous phase, which can be further confirmed by the XRD spectrum with no peaks shown in Fig. 2a. It is worth mentioning that the charge-trapping film in an amorphous state is favorable for the reliability of the memory device because charge loss via grain boundaries and defects at the CTL/SiO_2 interface induced by lattice mismatch can be avoided [3]. These defects along the grain boundaries or at the CTL/SiO_2 interface can enhance charge leakage and degrade the dielectric quality, and so are considered as reliability degraders, instead of effective traps for charge storage. Fig. 2b exhibits the Ti $2p_{3/2}$ spectrum as well as the curve-fitting lines. Each curve-fitting line is assumed to follow the general shape of Lorentzian–Gaussian function. The Ti $2p_{3/2}$ spectrum can be decomposed into two components, corresponding to Ti–O bonding in the $BaTiO_3$ film (~458.4 eV for Ti $2p_{3/2}$) [10] and Ti silicate at the $BaTiO_3/SiO_2$ interface (~459.0 eV for Ti $2p_{3/2}$) [11], respectively, where the Ti–silicate component displays a weak peak, indicating only a small fraction of $BaTiO_3$ transformed into silicate. This is consistent with the observation of the TEM image with no obvious interlayer at the CTL/SiO_2 interface. This non-stoichiometric Ti–silicate interlayer normally has a much smaller barrier height with respect to $BaTiO_3$ ($E_g \sim 3.3$ eV) as well as more defects compared with that of thermal SiO_2 tunneling layer ($E_g \sim 9.0$ eV) [6,10]. Consequently, an abrupt interface is desirable for good data retention properties because the charge-loss process related to the interlayer (e.g. defect-assisted tunneling) can be suppressed [12].

Fig. 3a depicts the 1-MHz $C–V$ hysteresis characteristics of the memory device with $BaTiO_3$ as CTL. Sweep starts from inversion region to accumulation region and back to inversion region again, corresponding to electron trapping and de-trapping respectively. As the sweeping voltage increases from ±8 V to ±12 V, the hysteresis window, defined as the difference of V_{FB} corresponding to the backward and forward $C–V$ curves, increases from 3.0 V to 7.6 V. The large window indicates a high trap density in the $BaTiO_3$ film. Moreover, the V_{FB} of the $C–V$ loop is more positive than the neutral V_{FB} (V_{FB} of the fresh device). Therefore, electrons trapped in the CTL during the backward sweeping are not completely removed after the forward sweeping, and thus a larger forward sweeping stress (−16 V → +12 V) is required to bring the $C–V$ curve back to the neutral position as shown in Fig. 3b. These phenomena should be associated with deep traps in the $BaTiO_3$ film [13] because electrons located in deep traps are more difficult to escape than those in shallow traps. As further increasing the forward sweeping stress (−18 V → +12 V), the V_{FB} slightly shifts towards the negative direction with respect to the neutral state, indicating only a small amount of hole traps in the $BaTiO_3$ film. Different from SiO_2 with covalent bonds, the ionic bonding in $BaTiO_3$ suggests its poor ability to remove a defect once created. It has been reported that oxygen can escape from $BaTiO_3$ during high-temperature annealing in a N_2 protective ambient, thus leading to oxygen vacancies [14]. Moreover, the Ti^{4+} sites in titanate can also act as acceptor levels for electron trapping [15]. Both of these reasons can contribute to high electron-trap density in the $BaTiO_3$ film. Considering the Ti $2p$ XPS spectrum with the fully oxidized Ti^{4+} state shown in Fig. 2b, it is believed that few oxygen vacancies are present in the $BaTiO_3$ film [16].

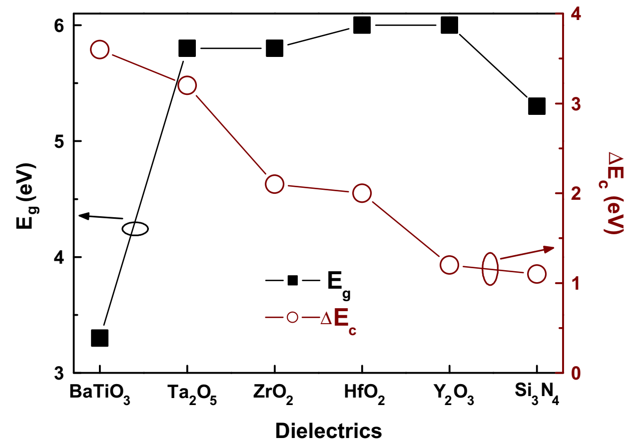

Fig. 1. Energy band-gap (E_g) and conduction-band offset with respect to SiO_2 (ΔE_c) of typical high-k dielectrics used as charge-trapping layer.

Table 1
Comparison of E_g and ΔE_c for typical high-k dielectrics used as charge-trapping layer.

	SiO_2	$BaTiO_3$	Ta_2O_5	ZrO_2	HfO_2	Y_2O_3	Si_3N_4
E_g (eV)	9.0	3.3	5.8	5.8	6.0	6.0	5.3
ΔE_c (eV)	0	3.6	3.2	2.1	2.0	1.2	1.1

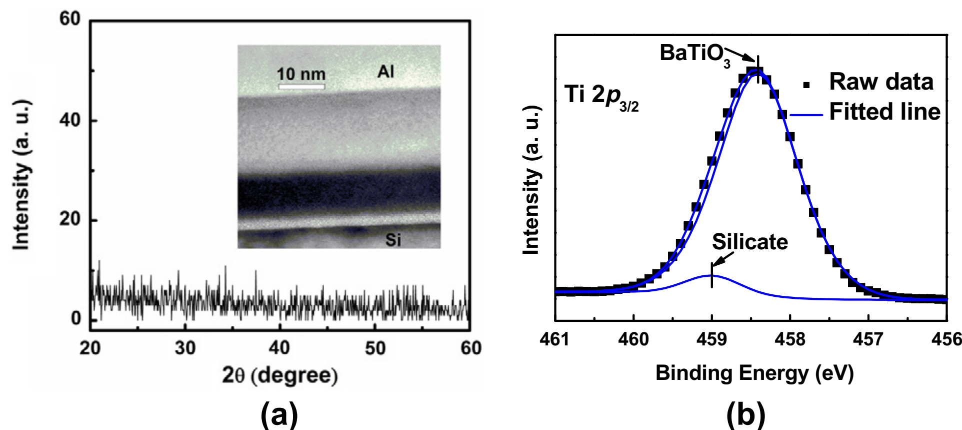

Fig. 2. (a) XRD spectrum of the $BaTiO_3/SiO_2$ (10 nm/2 nm) film on Si substrate. The XRD sample received the same thermal cycles as the MONOS capacitor. The inset shows the cross-sectional TEM image of the MONOS capacitor with $Al/Al_2O_3/BaTiO_3/SiO_2/Si$. (b) Ti $2p_{3/2}$ XPS spectrum of the $BaTiO_3/SiO_2$ stack on Si substrate.

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