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Integration of Si/SiGe HBT and Si-based RITD demonstrating controllable negative differential resistance for wireless applications

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Abstract

Si-based resonant interband tunnel diodes (RITD) were monolithically integrated with Si/SiGe heterojunction bipolar transistors (HBT) on silicon substrates effectively creating a 3-terminal negative differential resistance (NDR) device. We demonstrate that the room temperature NDR in the I_C–V_{EC} characteristics under common emitter configuration can be controlled by a third terminal which is the basis of the integrated circuit. The estimated NDR values from the DC I–V characteristics, assuming that the NDR is linear, can be varied from about −27.5 Ω to −180 Ω with respect to V_{CE} in the range of 0.96 V–1.16 V.

Keywords: Resonant interband tunnel diode; Heterojunction bipolar transistor; Negative differential resistance; Molecular beam epitaxy; Silicon germanium; Voltage controlled oscillator

1. Introduction

Low power consumption concurrently with high-speed performance is a key for next generation portable wireless applications including satellite communications. Devices such as tunnel diodes that exhibit negative differential resistance (NDR) in their current–voltage characteristics are very useful for circuit applications such as high-speed mixed signal and ultra-fast logic/memory with low power consumption. To date, applications using tunnel diodes that have been demonstrated include voltage-controlled oscillators [1,2], A/D converters [3,4], frequency dividers [5,6], sampling [7], memory [3,8], logic circuitry [5,9], etc. All these applications derive benefit from the intrinsic negative resistance of NDR devices which can also reduce power consumption by the reduction of circuit complexity and therefore device count. Furthermore, since the tunneling phenomenon is a majority carrier effect, the speed of circuits incorporating NDR devices can be much faster.

The most representative NDR devices are tunnel diodes. However, the utility of two terminal tunnel diodes themselves in circuits has several drawbacks such as input/output isolation, poor controllability, and vulnerability to the growth and fabrication procedure. Therefore, the use of transistors in conjunction with tunnel diodes by providing a third terminal with NDR devices will overcome the drawbacks described above and extend the useful range of NDR device based circuit applications. These types of

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hybrid circuits have already been demonstrated in many III–V compound semiconductor material systems mostly by the integration of unipolar resonant tunnel diodes (RTDs) with HBTs [1,5,10] or high electron mobility transistors (HEMT) [2–4,6]. However, despite the better performance of III–V-based NDR devices stemming from their different material properties such as a direct band gap, or large heterojunction band offsets, etc., such technology is not readily compatible with the mainstream platforms of complementary metal oxide semiconductor (CMOS) and Si/SiGe heterojunction bipolar transistor (HBT) technologies unless a suitable Si-based NDR device and compatible integration technology with existing Si-based CMOS or HBT devices is available.

The first Si-based tunnel diode integration was demonstrated using a Si/SiGe resonant interband tunnel diodes (RITDs) with a Si/SiGe HBT [11]. The resulting circuits showed the distinguishing characteristics of adjustable PVCR and PCD corresponding to the NDR by the control of the HBT base current. This enabled a 3-terminal NDR device and was the first report of a monolithic Si-based resonant bipolar tunneling transistor (RBT). This embodiment utilized interband tunneling versus the intraband tunneling via resonant tunneling diodes (RTD) utilized by III–V resonant tunneling transistors (RTT) [1,5,10].

This study extends the preliminary work of the authors [11], presenting an improved Si/SiGe-based RITD–HBT integration. The RITD–HBT integration discussed here shows the capability to adjust the NDR values by the control of the base current which is a third terminal of the integration as well as a greatly reduced series resistance. The estimated NDR values of the integrated RITD–HBT from DC I–V characteristics, assuming that NDR is linear, varies from about $-27.5\ \Omega$ to $-180\ \Omega$ with respect to V_{CE} in the range of 0.96 V–1.16 V. Two issues related to the improvement of the integration will be discussed: (1) reducing a large non-linear series resistance originating from the backward diode that is necessary to connect two bipolar devices in series without also introducing a reverse biased parasitic rectifying diode in between; (2) improving the gain of the SiGe HBTs. Included in this study is the load line analysis of the RITD–HBT integration for better understanding.

2. Structure design and process

The overall RITD–HBT structure, as shown in Fig. 1(a), consists of three intrinsic devices that are vertically stacked such that an n-on-p RITD is placed on top, an n–p–n HBT on bottom, and a p-on-n backward diode between the two devices.

A tandem of an n-on-p RITD on an n–p–n HBT is necessary for the RITD to modulate the current transport across the HBT emitter under forward active operation in the common emitter configuration (refer to Fig. 1: $V_{BE} > 0$, $V_{EC} > 0$, $V_{BC} > 0$) where the n-on-p RITD needs to be forward-based to make the NDR region appear. However, since both the RITD and HBT are bipolar devices, placing an n-on-p RITD directly atop the n-type of HBT emitter creates a parasitic diode between the two bipolar devices, which blocks current flow as it is reverse-biased under forward active operation. Therefore, inserted between the RITD and the emitter of the HBT was a backward diode which will be reverse-biased under HBT forward bias active operation in the common emitter configuration. The backwards diode effectively connects the top RITD and the bottom HBT appearing as a small series resistance for the vertically integrated RITD–HBT circuit.

The entire vertically integrated RITD–HBT structures were grown by low temperature molecular beam epitaxy (LT-MBE) using elemental Si and Ge in electron-beam sources on Sb-doped ($\rho = 0.008$–$0.018\ \Omega$ cm) Si(100) substrates. Two different n-type dopants, P and Sb were

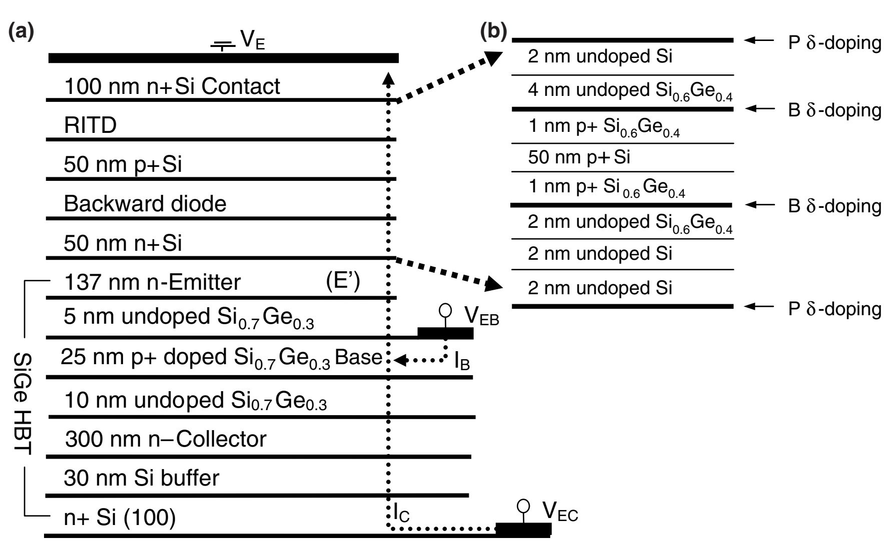

Fig. 1. The schematic of the RITD–HBT layer structure consisting of three intrinsic devices such that the n-on-p RITD is placed on top, the n–p–n HBT on bottom, and the p-on-n backward diode between the two devices. The detailed structure for the RITD and the backward diode is shown separately.