Available online at www.sciencedirect.com
SCIENCE DIRECT®
Solid-State Electronics 50 (2006) 1156–1163
SOLID-STATE ELECTRONICS
www.elsevier.com/locate/sse

Gate line edge roughness amplitude and frequency variation effects on intra die MOS device characteristics

Emad Hamadeh [a,b], Norman G. Gunther [a], Darrell Niemann [a], Mahmud Rahman [a,*]

[a] *Electron Devices Laboratory, Santa Clara University, Santa Clara, CA 95053, United States*
[b] *Applied Micro Circuits Corp. (AMCC), 215 Moffett Park Drive, Sunnyvale, CA 94089, United States*

Received 14 April 2006; accepted 19 April 2006

The review of this paper was arranged by A.A. Iliadis and P.E. Thompson

Abstract

Random fluctuations in fabrication process outcomes such as gate line edge roughness (LER) give rise to corresponding fluctuations in scaled down MOS device characteristics. A thermodynamic-variational model is presented to study the effects of LER on threshold voltage and capacitance of sub-50 nm MOS devices. Conceptually, we treat the geometric definition of the MOS devices on a die as consisting of a collection of gates. In turn, each of these gates has an area, A, and a perimeter, P, defined by nominally straight lines subject to random process outcomes producing roughness. We treat roughness as being deviations from straightness consisting of both transverse amplitude and longitudinal wavelength each having lognormal distribution.

We obtain closed-form expressions for variance of threshold voltage (V_{th}), and device capacitance (C) at Onset of Strong Inversion (OSI) for a small device. Using our variational model, we characterized the device electrical properties such as $\sigma_{V_{th}}$ and σ_C in terms of the statistical parameters of the roughness amplitude and spatial frequency, i.e., inverse roughness wavelength.

We then verified our model with numerical analysis of V_{th} roll-off for small devices and $\sigma_{V_{th}}$ due to dopant fluctuation. Our model was also benchmarked against TCAD of $\sigma_{V_{th}}$ as a function of LER. We then extended our analysis to predict variations in $\sigma_{V_{th}}$ and σ_C versus average LER spatial frequency and amplitude, and oxide-thickness. Given the intuitive expectation that LER of very short wavelengths must also have small amplitude, we have investigated the case in which the amplitude mean is inversely related to the frequency mean. We compare with the situation in which amplitude and frequency mean are unrelated. Given also that the gate perimeter may consist of different LER signature for each side, we have extended our analysis to the case when the LER statistical difference between gate sides is moderate, as well as when it is significantly large.

Keywords: Line edge roughness; Roughness amplitude; Roughness frequency; Roughness wavelength; Lognormal distribution; Thermodynamic-variational model; MOS device; Capacitance; Threshold voltage; TCAD

1. Introduction

Line edge roughness (LER) is a random fabrication process outcome. Common sources of random process outcomes for large devices such as dopant fluctuations, and oxide thickness have been studied in detail over the past few years. With the geometry of semiconductor devices approaching sub-50 nm dimensions, significant choices have been made concerning the lithographic technologies such as EUV, and water immersion optics. In addition, plasma etching produces sidewall striation which is a form of LER [1]. As consequences of such scaling, the quality of the resist lines and the corresponding polysilicon lines become of ever greater importance as the gate critical dimensions move into future technology nodes. Urgent attention is now being given to LER, which has been

* Corresponding author. Tel.: +1 408 554 4175; fax: +1 408 554 5474.
E-mail address: mrahman@scu.edu (M. Rahman).

0038-1101/$ - see front matter © 2006 Elsevier Ltd. All rights reserved.
doi:10.1016/j.sse.2006.04.031

identified as one of the grand challenges to the semiconductor industry according to ITRS 2003 publication [1–3].

The increasing role of gate LER of integrated circuit components in present and projected technology nodes in limiting pattern- and performance-related yield entitlements demands improvement in critical dimension SEM imaging, measurement and analysis [4–9]. In particular, LER affecting the gate dimensions of MOS devices and interconnects is random in both frequency and amplitude. Analysis based on consideration of the statistical nature of such fluctuations in process outcomes should take into account both sources of randomness. It becomes imperative for both product designers and process engineers involved in the development of such present and future technology nodes. The inherently 3-dimensional nature of devices of this size and the interaction of the fringe field and the quantum mechanical charge confinement effect further complicate the analysis.

In this work, using a thermodynamically based variational model, we have investigated the variation in capacitance and threshold voltage of a MOS device, as shown in Fig. 1. Our model expresses the minimization of the thermodynamic free energy of the device as a variational principle in the potential distribution.

The device LER is illustrated in Fig. 2, when (i) both frequency and amplitude variations are distributed log-normally, but are independent of each other, and when (ii) the means of the distributions are inversely related. The choice of lognormal distribution avoids the unphysical possibility of negative values of frequency or amplitude, and is clearly a good choice for the frequency distribution, as seen in Fig. 3. Making the means of the frequency and amplitude distributions to be inversely related eliminates the artificial mathematical possibility in our model of having infinite gate perimeter.

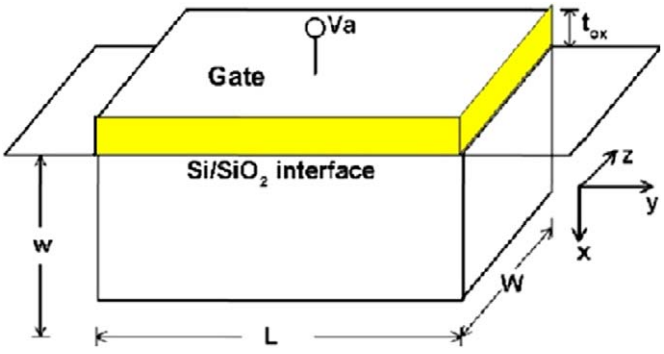

Fig. 1. Schematic of MOSCAP structure.

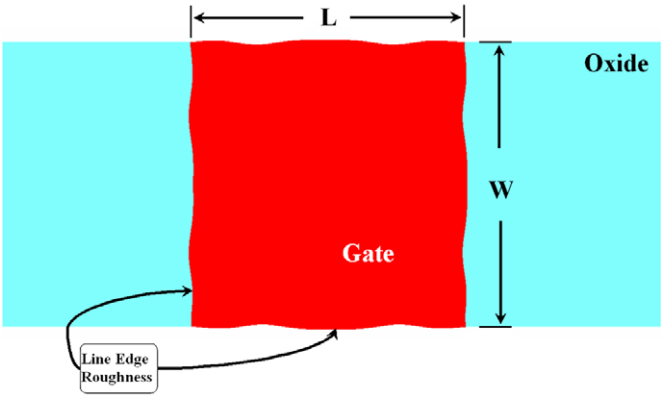

Fig. 2. Illustration of MOSCAP gate sides with LER.

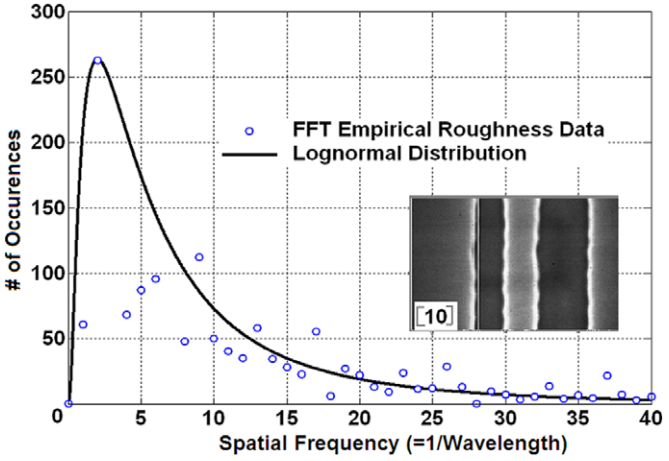

Fig. 3. FFT of roughness data together with lognormal pdf. The insert shows SEM of empirical LER [10].

It should also be noted that a rough gate has four rough sides, and the roughness of each side may be caused by different processes and have different statistical properties. The analysis presented here can easily be extended to accommodate the inclusion of the additional frequency and amplitude random variables which would be needed to address this situation. In Section 6, we model a case of a gate with two rough sides, such that each side has its own spatial frequency distribution.

Meaningful TCAD simulation of very small devices incorporating rough dimensions will serve to benchmark the results we obtain using the more flexible thermodynamically based methods. However, these benchmarks are difficult because of the need to incorporate the statistical nature of roughness.

The rest of the paper is organized as follows: In Section 2, we discuss the statistical frequency and amplitude characteristics which are used to describe LER. In Section 3 we derive closed-form expressions for the deviations of threshold voltage and capacitance at onset-of-strong-inversion (OSI) in terms of the device parameters and the statistical characteristics of LER. In Section 4 we compare results of numerical simulations and TCAD with those obtained by our model. Next, in Section 5, we present results obtained using our model for such cases as, (i) when the LER amplitude and frequency are independent of each other, and (ii) when they are related. In Section 6, we present the case when gate sides have different roughness. We conclude our findings in Section 7.