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(110) and (100) Sidewall-oriented FinFETs: A performance and reliability investigation

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ABSTRACT

The performance and reliability of (100) and (110) sidewall, silicon-on-insulator (SOI) FinFETs with a Hf-based gate dielectric were evaluated. Unlike the typical planar MOSFET mobility orientation dependence, (110) FinFET sidewalls do not impair electron mobility and result in good short channel performance compared to (100) FinFET sidewall devices. Hot carrier injection (HCI) degradation was also investigated with nMOS and pMOS high-κ FinFETs on both sidewall surface orientations. Impact ionization at the source, as well as at the traditional drain side, was found to enhance HCI degradation when gate voltage (V_g) = drain voltage (V_d). The degradation becomes more pronounced as the gate length decreases, with a negligible dependence on substrate orientation. However, the orientation dependence of negative bias temperature instability (NBTI) on FinFETs demonstrates that the (110) orientation is slightly worse than (100). The kinetics of $\Delta N_{IT}(t)$ under negative bias stress conditions suggests the interface trap density (N_{IT}) is generated by a mechanism similar to that in planar devices.

1. Introduction

To meet the current and upcoming performance and reliability needs projected by the International Technology Roadmap for Semiconductors (ITRS) [1], the gate dielectric stack [2–6], induced strain effects [7–20], and substrate material and crystallographic orientation effects [15,21–31] were investigated on planar transistors. In addition, three-dimensional (3D) device structures are also under evaluation because they are attractive replacements for conventional planar silicon devices in technologies as they scale below the 22 nm node due to the increased need for short channel electrostatic control at short gate lengths. These 3D structures, also known as multi-gate FETs (MugFETs), have the gate wrapped around a narrow "fin" that enables excellent short channel control of the transistor (see Fig. 1). FinFETs can be fabricated with either a (110) sidewall surface or (100) sidewall. The crystal orientation of these fin sidewalls, which sometimes incorporates strain, can have an impact on performance and reliability [32–49].

In planar CMOS technologies, orientation-dependent mobility enhancement has been demonstrated using a hybrid orientation technology (HOT) [21,22,24]. Here, hole mobility (μ_{eff}) increases significantly when the channel orientation changes from Si (100) to Si (110). However, this change also severely degrades electron mobility. HOT, therefore, needs to take advantage of hole μ_{eff} on Si (110) and electron μ_{eff} on Si (100), which adds to the complexity of integration approaches.

Our work demonstrates that (110) nMOS FinFET devices do not experience the same mobility degradation as planar nMOS, thereby mitigating the need for orientation-dependent CMOS FinFETs to enhance μ_{eff} [50]. Since mobility was evaluated on long channel devices, performance verification is required to confirm similar performance characteristics for appropriate device dimensions. Moreover, the implications of sidewall surface orientation on reliability issues such as hot carriers [51,52] and bias temperature instability [53–55] must likewise be addressed. The surface orientation or 3D fin structure may be more susceptible to degradation during stress when compared to planar devices. Possible causes include the Si interface bonds that can break [56] in the (110) plane or structural properties that impact reliability differently than in planar devices.

In this work, we evaluate the dependence of FinFET crystallographic sidewall orientation on performance (i.e., mobility and I_{on}/I_{off}) and reliability, investigating hot carrier injection (HCI) and NBTI.

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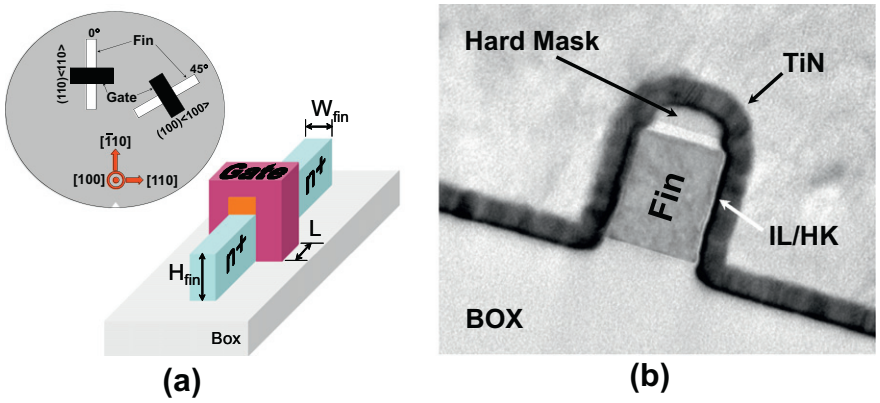

Fig. 1. (a) FinFET devices with (110) or (100) sidewall orientations on the same wafer can be formed with two sidewall orientations by fabricating FinFETs rotated 45° to obtain (100) where the double-gate FinFET structure (nMOS example) on SOI has key fin dimensions identified: $H_{fin} \sim 40$ nm, and $W_{fin} \sim 20$ nm. (b) Cross sectional TEM image of a typical FinFET structure used in this work.

Table 1
FinFET device structures used in this work.

FinFET gate stack
1 nm SiO_2/2 nm HfO_2/TiN
1 nm SiO_2/2 nm HfO_2 /TiN (with Tensile CESL)
1 nm SiO_2/2 nm HfO_2/TiN (with doped fin body)
2.5 nm SiO_2/Poly Si

2. Experimental

2.1. Fabrication

Silicon-on-insulator (SOI) FinFETs were processed with channels formed on (100) and (110) planes. Neutral stress (100) SOI substrates were patterned using 193 nm lithography to produce arrays of fins with an aspect ratio of ~2:1. Hafnium-based high-k (~2 nm) and mid-gap metal gate (~10 nm) with a poly cap formed the gate stack. The spacer was deposited immediately after gate patterning without extension implants where nMOS and pMOS devices were distinguished by separate implant and anneal processes with Ni-based salicide completing the front-end processing. Standard back end-of-line (BEOL) processing using an unstressed contact etchstop layer (CESL), interlevel dielectric (ILD), contact plugs, and metallization completed the fabrication sequence. Fig. 1a illustrates the result of this process where a 3-D FinFET transistor is formed with a gate that envelops the fin and a hard-mask on top of the fin to decouple the top surface from device operation on the device sidewall surfaces (Fig. 1b). Customarily, devices are processed with a (110)⟨110⟩ sidewall orientation, but rotating FinFETs 45 degrees on the same wafer creates transistors with an (100)⟨100⟩ orientation. The process flow was modified to fabricate SiO_2/poly gate stacks and incorporate fin body doping or tensile CESL (Table 1). The gate first, bulk-Si planar MOSFETs used for comparison, which had the same Hafnium-based high-k and TiN metal gate (HK/MG) stack [22], were processed with channels formed on (100) and (110) surfaces. The finFET devices had a fin height of ~40 nm with various fin widths (~25 nm typical unless denoted otherwise) and various gate lengths.

2.2. Measurements

2.2.1. Mobility and short channel performance

For mobility extraction, split capacitance–voltage (split *C–V*) [57] measurements at 100 kHz were taken on FinFET structures with 200 parallel fins that are ~40 nm high, and a 10 μm gate length (L_g). From these same structures, drain current–gate voltage (I_d–V_g) measurements were performed in the linear regime. Mobility was extracted from (1) and (2) using split *C–V* for Q_{inv} and channel conductance ($g_d = \Delta I_d/\Delta V_d$) from differential I_d–V_g measurements at 20 mV and 40 mV [36,58],

$$\mu_{\text{eff}} = \frac{\Delta I_d}{\Delta V_d \frac{W}{L}(Q_{\text{inv}})} \tag{1}$$

$$W = M \cdot 2 \cdot H_{\text{fin}} \tag{2}$$

where L is the gate length; the width (W) is defined by the number of fins (M) times the product of the height (H_{fin}) of the two fin sidewalls; and Q_{inv} is the inversion charge (C/cm^2) from the integration (i.e., area under the curve) of the split *C–V* data. When necessary, the drain current was corrected for gate leakage using [59]. Split *C–V* and I_d–V_g measurements also included temperature dependence (20 K–300 K) on the different sidewall channel surface orientations with subsequent μ_{eff} extraction and modeling.

Standard I_d–V_d measurements along with saturation current (I_{dsat}) data were collected from multiple short channel lengths to generate $I_{\text{on}}/I_{\text{off}}$ performance plots for the differently oriented FinFETs.

2.2.2. Hot carrier injection

HCI on (110) and (100) channel surfaces was carried out on nMOS and pMOS FinFETs of different gate lengths (90 nm, 110 nm, 250 nm, as drawn). In the HCI methodology, a stress bias is applied to the gate at a value typically above the operation voltage to accelerate degradation while applying a bias to the drain at typical values of $V_d = V_g$ or $V_d = V_g/2$. When exposed to this type of stress, devices become susceptible to interface trap generation and hot electron injection (from impact ionization) into the gate dielectric at the drain side of the device. The stress bias condition was set such that V_g–V_t was 1.3, 1.5, or 1.7 V with interspersed source-to-drain (S/D) and reverse drain-to-source (D/S) I_d–V_g sense measurements to monitor the shift in threshold voltage (ΔV_t) and I_{dsat}.

2.2.3. Negative bias temperature instability

NBTI stress measurements were carried out for 10,000 s at 125 °C on (110) and (100) pMOS FinFETs. NBTI occurs in pMOS devices that are stressed with negative bias at elevated temperatures; it increases device V_t and off-state leakage while concurrently degrading I_{dsat} and transconductance (g_m) [60]. The stress bias condition was set such that the V_g–V_t was 1.3, 1.5, or