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Low-frequency noise in high-k $LaLuO_3$/TiN MOSFETs

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ABSTRACT

Low-frequency noise (LFN) characterization of high-k $LaLuO_3$/TiN nMOS transistors is presented. The experimental results including the noise spectrum and normalized power noise density and mobility are reported. The noise results were successfully modeled to the correlated number and mobility fluctuation noise equation. High-k dielectric devices show lower mobility and roughly one to two orders of magnitude higher low-frequency noise which is comparable to the hafnium based oxide layers. The implementation of higher-k $LaLuO_3$ seems to be a suitable candidate to the trade-off between equivalent oxide thickness scaling and low frequency noise.

1. Introduction

Advanced gate stacks are promising materials in order to enable the progress of MOSFET scaling [1]. Applying a high-k dielectric reduces the equivalent oxide thickness (EOT) while keeping the leakage current low. Hafnium based dielectrics with $k\sim22$ have been used as high-k dielectrics successfully in the CMOS technology [2]. However, in order to keep the scaling trend ongoing the implementation of higher-k dielectrics with a suitable metal gate is inevitable. A good alternative is Lanthanum Lutetium oxide ($LaLuO_3$) with $k\sim30$ which promises EOT values lower than 1 nm with a low leakage current [3]. This high-k material is reported to have excellent thermodynamic stability up to $\sim$1000 °C which can be an advantage in the gate-first process. Furthermore it has an optical band gap around 5.2 eV with a symmetrical 2.1 eV conduction and valence band offset to Si. Previous studies on $LaLuO_3$ includes the integration of $LaLuO_3$ on SOI MOSFETs [4], mobility studies on these transistors [5] investigating the trapping/detrapping of charges on $LaLuO_3$ MOS capacitor [6], deposition on Germanium-on-insulator substrates [7] and deposition on AlGaN/GaN MISHEMTs [8]. Although advantageous, there are still main issues that need to be considered in high-k devices. The high-k dielectric introduces more interface and bulk traps leading to instability in threshold voltage, mobility degradation and $1/f$ noise level increment. The reported number of negative trap states per unit area for a $LaLuO_3$ MOS capacitor is $N_t = 2.2 \times 10^{11}$ cm^{-2} and for positive charges $N_t = 6.6 \times 10^{11}$ cm^{-2} [6].

The main focus of this work is on low-frequency noise since excessive level of LFN noise can be a major concern in stability and reliability of electronic circuits. According to table RFAMS1 of the ITRS roadmap [1], the $1/f$ noise needs to meet more strict requirements for RF and analogue mixed signal CMOS technology. This topic is even more challenging in the new technology devices as this noise increases with device scaling.

The low-frequency noise in MOSFETs which is investigated through the drain current can be due to carrier number fluctuations, mobility fluctuations or a result of both. Based on comprehensive studies in this area, it is considered that $1/f$ noise can be analyzed in MOSFETs and modeled considering the mechanisms originating the noise.

In this work, for the first time, the low-frequency noise in high-k $LaLuO_3$/TiN metal gate n-type transistors is measured and discussed. Additional studies on the mobility helped determine the physical explanation behind the source of noise in these devices better.

This article is organized as followed: In Section 2 the device fabrication and experimental details are explained. The results of low-frequency noise and mobility measurements are reported in Section 3 followed by fitting a noise model to the results for these devices. Finally, the conclusions are summarized in Section 4.

2. Fabrication and experimental details

2.1. Device fabrication

These devices were fabricated on a 30 nm thick SIMOX SOI substrates. The thickness of silicon was reduced through sacrificial dry

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Table 1
Combination of the gate stacks.

Wafer	SiO_2 thickness (nm)	$LaLuO_3$ thickness (nm)	TiN thickness (nm)
Reference	5	NA	20
High-k1	5	6	20
High-k2	NA	6	20
High-k3	NA	20	20

oxidation and HF wet etching. This was followed by MESA etching to define active areas. The composition of gate stacks is different among the wafers and is summarized in Table 1. The reference wafer has no high-k dielectric layer. In other wafers, the high-k dielectric with different thicknesses (t_{hk} = 6 nm, 20 nm) was deposited by MBE. In one of the wafers a 5 nm interfacial oxide layer was placed beneath the high-k layer. In the next step, TiN metal gate was deposited by sputtering on all wafers followed by deposition of in situ phosphorus doped poly-Si (t_{poly} = 150 nm). After the gate dimensions were defined through I-line lithography, poly-Si/TiN etch was performed. PtSi Schottky-barrier source/drain was formed and implanted with arsenic for nMOSFETs. To enable dopant segregation at the PtSi/Si interface, RTA at 700 °C was carried out. LTO oxide deposition, contact hole patterning, metallization and FGA (10% H_2 in N_2 at 400 °C for 30 min) finalized the fabrication process.

2.2. Experimental

The low-frequency noise measurements were carried out on nMOS devices on four different wafers described above. Different gate lengths (L_G = 0.35, 0.5, 1 μm) and gate widths (W_G = 10, 50 μm) were investigated. The gate voltage was stepped from subthreshold to strong inversion region at two different drain biases V_{DS} = 50 mV (linear region) and V_{DS} = 1 V (saturation region). The measured frequency range was chosen to be between 1 and 100 Hz. The low-frequency noise measurement setup consists of a Programmable Biasing Amplifier (PBA) with an external low noise power supply and a spectrum analyzer.

For the mobility measurements, the drain conductance method is used and N_{inv} is obtained from split-CV measurements. The mobility parameter was extracted for the four different wafers. The largest area devices (W = 50 μm, L = 3 μm) were chosen for this measurement.

3. Results and discussion

3.1. Mobility

The channel mobility in MOSFETs is a critical parameter which has been vastly studied and successfully modeled for standard MOSFETs. However, there are additional factors limiting the mobility in high-k MOSFETs leading to a lower mobility in these devices. The mobility degradation is mainly originated from scattering due to charges in the high-k and at the interface, surface roughness scattering, remote Coulomb scattering and remote phonon scattering [9–11]. The latter appears only in high-k transistors.

The extracted mobility parameters versus the inversion charge density are plotted in Fig. 1. The mobility degrades from the reference wafer to high-k3 due to increased number of traps as expected. Phonon scattering seems to be the dominant scattering mechanism in the reference and high-k1 wafer. A large variation in mobility is observed in the high-k1 devices, which could be related to unstable interface between interface silicon dioxide and the deposited high-k on top. This is also seen in the threshold voltage shift among different dies of this wafer. The reference wafer shows stable mobility behavior and threshold voltage. Only limited statistics could be achieved for high-k2 and high-k3 wafer due to high gate leakage current.

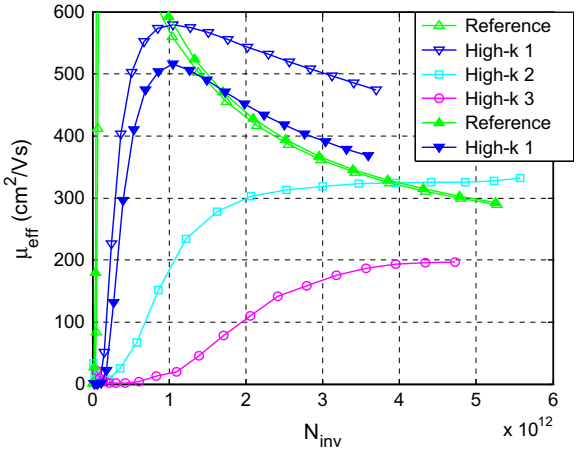

Fig. 1. Mobility versus inversion charge density measured on W = 50 μm, L = 3 μm n-type devices.

3.2. Low-frequency noise

The drain current noise spectrum between 1 and 100 Hz for an n-type LaLuO3/TiN MOSFET is shown in Fig. 2. The gate voltage ranges from V_{GS} = 0 V to 1.6 V. The threshold voltage (V_T) of this device was around 0.5 V which was extracted through measurements of the slope at maximum g_m of I_D–V_{GS} curve. The noise level follows the gate bias clearly. A similar $1/f^{\gamma}$ behavior is shown in all the devices ($0.8 < \gamma < 1.2$). However these devices seem to show an obvious $1/f$ behavior at gate biases higher than the threshold voltage while a less steep slope is observed at lower gate voltage biases which shows the background noise.

To verify the reproducibility of the data, a device to device comparison is investigated. This comparison for n-type devices is shown in Figs. 3 and 4, for the reference wafer and high-k1 wafer respectively. These plots show the normalized drain current noise ($S_I D/I_D^2$) measured at f = 10 Hz versus the drain current. The measurements were performed at two different drain bias voltages which is observable in the plots. As depicted, the two plots overlap well especially in the strong inversion region. In Fig. 5, the devices are compared in a geometrical point of view. The $1/f$ noise is

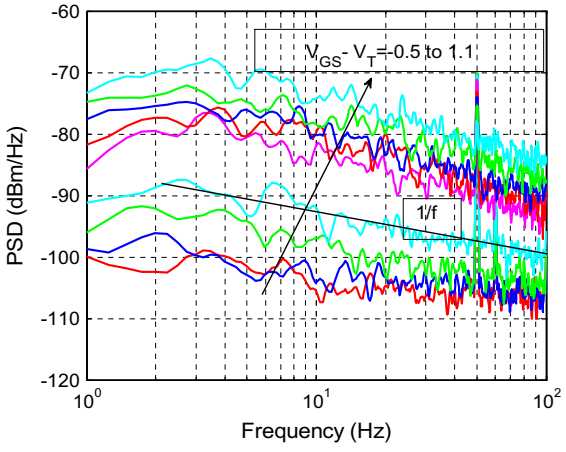

Fig. 2. N-type device W = 10 μm, L = 0.5 μm noise spectrum extracted from the reference wafer.