Solid-State Electronics 73 (2012) 32–36

Contents lists available at SciVerse ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

Light triggered 4H–SiC thyristors with an etched guard ring assisted JTE

Nicolas Dheilly [a,*], Dominique Planson [a], Gontran Pâques [b], Sigo Scharnholz [b]

[a] Université de Lyon, INSA de Lyon, Ampere Lab, UMR 5005, 69621 Villeurbanne, France
[b] French-German Research Institute of Saint-Louis (ISL), 68300 Saint-Louis, France

ARTICLE INFO

Article history:
Received 7 July 2011
Received in revised form 10 January 2012
Accepted 13 February 2012
Available online 14 April 2012

The review of this paper was arranged by Prof. S. Cristoloveanu

Keywords:
Silicon Carbide
Light triggered thyristor
Etched termination
Guard rings assisted JTE

ABSTRACT

In this paper, an original termination, the etched guard ring assisted junction termination extension (JTE), is demonstrated on 4H–SiC light triggered thyristors. The termination structure, designed with finite element simulations, is detailed and particular attention is paid to the sensitivity to etching depth uncertainties. The fabrication processes and the electrical characterization of the devices are described. A blocking voltage of 6.3 kV is attained, validating the principle of the termination. Switching and quasi static on-state measurements are also performed to investigate the functionality of the thyristors.

1. Introduction

Power electronics and pulse power systems in particular require ever lighter, more compact and more efficient semiconductor switches. To further improve the performances of the power devices, the use of wide bandgap semiconductors is a very promising solution. Among these, 4H–Silicon Carbide (SiC) has very interesting properties such as its large bandgap (3.26 eV) and its very high critical field (2–3 MV/cm). Moreover 4H–SiC fabrication technology is one of the most mature among all wide bandgap materials.

Pulse power systems as they are developed by ISL [1] and others [2,3] require devices sustaining high current pulses and voltages in the range of 5–10 kV. Thanks to the conductivity modulation in its drift layer, the thyristor is the best suited device to assess these requirements. To reach such high blocking voltage, the optimization of the device edge termination is essential. The latter 4H–SiC thyristor demonstrators found in the literature use systematically, as edge termination, a mesa combined with single or multiple implanted junction termination extension (JTE) [4–6]. However, ion implantation causes serious damage to the crystal structure that is only partially recovered with the activation annealing. Moreover, the implantation process is difficult to control precisely, resulting in uncertainties in the final active dopant concentration. Implantation free SiC bipolar devices with good results have already been fabricated with single or multiple etched JTE [7,8].

Compared to a classic electrical triggering with a gate contact, the optical triggering provides a galvanic isolation of the driver. Light triggering also simplifies systems when several devices are needed in parallel or in series, eliminating symmetry and inductance issues in the gate current path. Moreover one possible drawback when abandoning ion implantation in BJTs or thyristors could be a more resistive gate contact, the problem of which is no issue in light triggered thyristors (LTTs).

In the first part of this paper, the design of an implantation-free guard ring assisted etched JTE using finite elements simulations is detailed. Then the fabrication of optically triggered SiC thyristors with such termination is described. The blocking and conducting forward characteristics of these devices are finally presented.

2. Design of the termination

2.1. Simulation description

Sentaurus TCAD software was used for the design of the termination. Ionization coefficient parameters are necessary to determine the blocking voltage of the different structures with the simulation tool. In this work, those published by Konstantinov et al. [9] were taken. The hole ionization integral equal to one is the criterion chosen to define the blocking voltage of the simulated devices.

The starting material for the simulation and the fabrication of the devices is a N-type substrate with four epilayers (Substrate N+/P/P−/N/P+) (Fig. 1). The forward blocking voltage is held by

* Corresponding author.
E-mail address: nicolas.dheilly@insa-lyon.fr (N. Dheilly).

0038-1101/$ - see front matter © 2012 Elsevier Ltd. All rights reserved.
http://dx.doi.org/10.1016/j.sse.2012.02.007

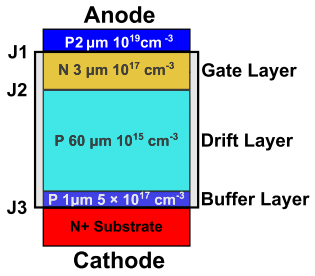

Fig. 1. Starting material for the fabrication of the thyristors.

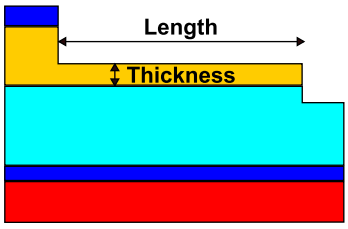

Fig. 2. Schematic of the simple etched JTE termination.

the junction J2. To simplify the computations, only the gate, drift and buffer layers (surrounded in Fig. 1) are considered in the simulation. The entitlement of the one-dimensional junction J2 as determined by our simulation is 8140 V.

2.2. Simple etched JTE

The simple etched JTE is formed by two etching steps that define its inner and outer edges. A schematic view of this termination is shown in Fig. 2. The length and thickness of the JTE are the parameters to be adjusted in order to obtain a device with a high blocking voltage. The MESA etching at the outer edge of the JTE was set to a level 1 µm deeper than the junction between the gate and drift layer. A SiO_2 passivation with a thickness of 1 µm was considered in the simulations. The dose of the JTE, is defined by the gate layer doping concentration and the JTE thickness. The gate being moderately doped (10^{17} cm^{-3}), the JTE dose can be quite precisely adjusted with the etching depth. The dose is the remaining thickness multiplied by the doping of the gate epi-layer.

Fig. 3 shows the simulated blocking voltage of the simple etched JTE versus its thickness, for various JTE length. On the right axis is the termination efficiency, which is the ratio in percent between the blocking voltage of the terminated structure and the one of the unidimensional structure (8140 V for our epilayers). The maximum termination efficiency of the simple etched JTE is 88%. This maximum is reached for a thickness of 0.9 µm and a JTE longer than 125 µm. The blocking voltage drops abruptly from 7100 V to 3800 V if the thickness of the JTE goes from 0.9 to 0.95 µm. Indeed, for this latter value, the JTE dose is too high to be fully depleted when the junction is reverse biased. Consequently, no spreading of equipotential lines occurs horizontally across the JTE, resulting in an inefficient termination. This also explains why the length of the JTE has no influence on the blocking voltage for a JTE thicker than 0.9 µm.

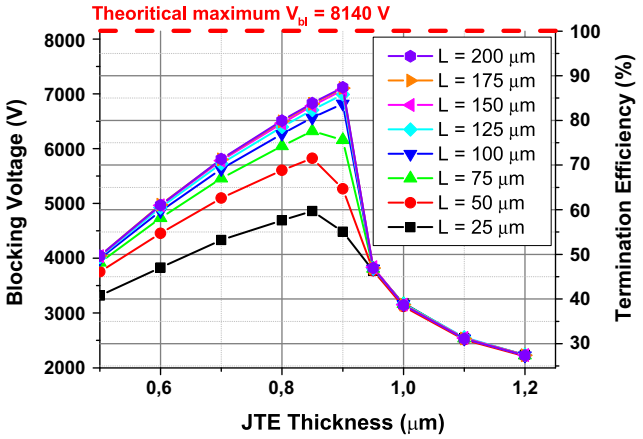

Fig. 3. Blocking voltage versus the JTE thickness for various JTE length.

The simple etched JTE has no outstanding performances and is very sensitive to the uncertainties on the etching depth. In fact, a precision of ±0.05 µm on the etching process is needed to guarantee 80% termination efficiency. As the RIE (Reactive Ion Etching) process is hard to control so accurately, an other edge termination structure has been considered, the guard ring assisted etched JTE.

2.3. Guard ring assisted etched JTE

The guard ring assisted JTE was first demonstrated on diodes by Perez et al. [10]. This edge termination was realized by ion implantation and the spacing between rings was constant. The principle of this termination is to include guard rings in the JTE. The guard rings, that have higher dose than the JTE, induce electric field peaks which help in the distribution of the voltage across the edge termination. A termination based on this structure, with variable spacings and formed with etching process steps, is studied hereafter.

Fig. 4 shows a schematic view of the termination structure. The starting point for the optimization was a 0.5 µm thick and 200 µm long JTE which has a termination efficiency of 50%. Guard rings were then added successively in the JTE to enhance the blocking voltage. Their width and thickness were set constant to 10 and 2 µm, respectively. Considering the fabrication process, these rings will be patterned using a thick photoresist mask. Consequently, the sidewall of the etched rings will be inclined. An angle between the horizontal surface and the sidewall of 30° was taken for the simulations. Compared to a vertical sidewall, an inclined one reduces significantly the electric field at the edge of the rings in the semiconductor and the passivation layer.

The optimization approach of the structure is the following. The termination with a single ring is first simulated, varying the space d_1 between the active area and the ring. Once the optimum distance d_1 has been found, another ring is included in the JTE. As shown in Fig. 4, the optimized spacing d_1 is the distance between the first outermost ring and the second one. The spacing d_2 between the active area and the second ring is then adjusted to get the highest possible blocking voltage. The method is the same for the next rings. This optimization ends when the spacing d_n is too short for the resolution of the lithographic process. The resolution of our lithographic process being 2 µm, the optimization of this termination lead to a JTE assisted by 6 rings with spacings from d_1 to d_6 being 8, 6, 5, 4, 3, and 2 µm long.

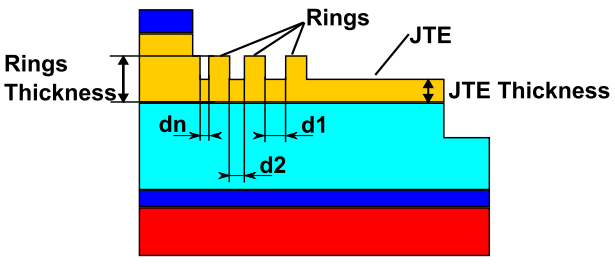

Fig. 4. Schematic of the etched guard ring assisted JTE.