Solid-State Electronics 73 (2012) 51–55

Contents lists available at SciVerse ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

Time-dependent device characteristics in InAs/AlSb HEMTs

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ARTICLE INFO

Article history:
Received 12 November 2011
Received in revised form 23 February 2012
Accepted 22 March 2012
Available online 22 April 2012

The review of this paper was arranged by Prof. E. Calleja

Keywords:
InAs/AlSb
High-electron-mobility transistor (HEMT)

ABSTRACT

This study investigates the device characteristics of InAs/AlSb HEMTs subjected to different periods of time storage in atmospheric ambiance after fabrication. Devices that have undergone 6 months of storage exhibit an increase of saturation drain current (I_{DSS}), increase of peak transconductance, decrease of gate leakage (I_G) and shifts of threshold voltage (V_{th}). The charge trapping effect was investigated by using a pulsed I_D–V_{DS} measurement, indicating that surface traps or defects were generated in the device that had undergone a 6-month storage. The decrease of I_G and shifts of V_{th} were found to correlate with material oxidization in the gate to the channel region, where an oxygen signal was detected by energy-dispersive analysis with X-ray (EDAX). Variances of gate capacitances (C_{gs}) extracted by the small-signal model were also used to justify the shifts of V_{th}.

1. Introduction

In the continuing pursuit of Moore's Law, III–V semiconductors are the most promising candidates for replacing Si to develop further high-speed, low-power logic applications. InAs/AlSb quantum wells, having a high electron mobility of 30,000 $cm^2/V\,s$ [1] and a high peak velocity of 4×10^7 cm/s [2] at room temperature, are successfully applied to develop low-noise and low operation voltage devices. Bergman et al. [3] achieved a simultaneously high peak RF g_m (~1500 mS/mm at 500 mV drain bias), peak f_T and peak f_{max} ~235 GHz at a drain bias of 300 mV, and f_T, f_{max} values exceeding 100 GHz with a drain bias of only 100 mV. Additionally, the InAs/AlSb HEMT has achieved equivalent high-speed figures of merit performance at 5–10 times lower dissipation than the GaAs or InP material system [4]. A single-ended low noise amplifier (LNA) demonstrated 1.5 dB typical noise figure with an associated gain of 25 dB from 1–16 GHz at a low dc dissipation of 16 mW [5]. However, the chemical instability of antimonide materials is a concern, which makes AlSb easily oxidized in air [6] and vulnerable to base attacks on the antimonides [7]. Prior study reported that adding In in the AlSb barrier helped to improve the device stability after 80 weeks [8]. A chemically stable $In_{0.5}Al_{0.5}As$ cap layer is therefore widely utilized on the device's surface to protect the underlying antimonide materials [4,9–11]. Another feasible way to reduce degradation of antimonide materials is passivation technology. Device passivation is a required or necessary process for circuit applications and is implemented not only to protect the devices from atmospheric and environmental chemical attacks and reduce the defect (trap) density on the device's surface, but also to produce the dielectric layer of a capacitor for monolithic microwave integrated circuit (MMIC) application. Suitable passivation technology can enhance the performance, reduce gate leakage of the device, and obtain excellent thermal stability [12–15].

In order to further investigate how the quality of epitaxial layers affect device characteristics, we fabricated the InAs/AlSb HEMTs using a conventional mesa process without additional passivation technology and continually observed the device from as-processed to 6 months later. Conventional dc, pulsed I_D–V_{DS} measurements, energy-dispersive analysis with X-ray (EDAX) and small-signal model of HEMT were all discussed.

2. Epitaxial materials and device fabrication

The InAs/AlSb HEMT epitaxial materials were grown by solid-source molecular beam epitaxy (MBE) on a semi-insulating (001) GaAs substrate. Native oxides of the substrates were first desorbed at 610 °C for 10 min under an As_2 flux before epitaxial materials were grown. Growth was initiated with a 0.2 μm-thick smoothing layer of GaAs and a 10 nm-thick transition layer of AlAs just before the AlSb buffer layer. The AlSb buffer layer, grown at 540 °C, was 1.2 μm thick and served primarily to accommodate a ~7% lattice mismatch between the (Al, Ga) Sb/InAs system and the GaAs substrate. Following the AlSb buffer layer, a 0.3 μm-thick $Al_{0.7}Ga_{0.3}Sb$ layer, grown at 500 °C, provided a stable surface during the device mesa isolation step [16]. The active layers were grown at 470 °C and consisted of a 10 nm AlSb bottom barrier layer, a 13 nm InAs channel layer, and a 11 nm AlSb top barrier layer. Finally, a

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0038-1101/$ - see front matter
http://dx.doi.org/10.1016/j.sse.2012.03.006

0.6 nm GaSb, a 5 nm $In_{0.5}Al_{0.5}As$ and a 2 nm InAs were grown as a cap at the surface [11]. An InSb-like interface was applied at the InAs–AlSb heterojunction to optimize the electron mobility in the InAs channel [17]. A planar tellurium (Te) modulation doping sheet was applied 5 nm above the channel layer for modulating carrier density. Room-temperature Hall measurement of the as-grown wafers revealed electron mobility of ~18,600 $cm^2/V\,s$ and a sheet carrier concentration of $\sim 3.35 \times 10^{12}\ cm^{-2}$.

The fabrication of the InAs/AlSb HEMT started with the formation of Pd/Ti/Pt/Au source and drain ohmic contacts. The Mesa was then defined using inductively coupled plasma reactive ion etching (ICP-RIE) which stopped in the $Al_{0.7}Ga_{0.3}Sb$ layer. Following the fabrication of Ti/Pt/Au Schottky gates, metallic probing pads of Ti/Au were finally made. TLM measurements yielded a contact resistance of 0.07 Ω-mm. The gate length and width of the device were 2 μm and 2 × 50 μm, respectively. The distance between gate and drain is 2 μm, and the distance between drain and source is 6 μm. Fig. 1 schematically depicts the cross-sections of the device.

3. Results and discussions

Figs. 2 and 3 plot the typical output and transfer characteristics of 2-μm gate length InAs/AlSb HEMTs that had undergone different periods of time storage in the atmospheric ambiance with humidity controlled around 35% at room temperature. The devices that had undergone 3- and 6-month storage had a higher saturation drain current (I_{DSS}), a higher peak transconductance ($g_{m,peak}$) and a lower source-drain on-resistance (R_{on}) than the as-processed one without any storage time. The I_{DSS} and $g_{m,peak}$ increased from ~517 mA/mm and ~750 mS/mm to ~575 mA/mm and ~1300 mS/mm at V_{DS} = 0.4 V. The high transconductance was due to impact-ionization effects [18]. Different types and densities of surface traps may vary the electric field distribution across the channel and thus the effects of impact-ionization in bias [19,20]. For comparison, the device that had undergone a 6-month storage had lower sheet resistance (R_s) than the as-processed one, which was a decrease from 98.8 Ω/□ to 94.7 Ω/□ by transmission line model (TLM) measurement. These dc and R_s characteristics may suggest that the device that had undergone 6-month storage had induced different types and densities of surface traps, which caused carrier concentration depletion, various charge trapping effects and electric field distribution across the channel [19,20].

Fig. 4 compares the sub-threshold drain and gate characteristics of the as-processed device with those of the devices that have undergone 3 or 6-month storage. The threshold voltage (V_{th}) at drain currents of 1 mA/mm shifted from ~−1.2 V of the as-processed device to ~−1.8 V of the other two devices. Furthermore, the increase in on-state drain currents, I_{on}/I_{off} ratios are raised from ~722 for the as-processed device to ~1361 for those that had undergone 6-month storage. Fig. 5 compares the Schottky gate leakage current of the devices that had undergone different periods of time storage. The devices that had undergone 3- or 6-month storage show lower gate leakage current than the as-processed one with gate bias of −1.3 V. In the epitaxial structure, AlSb is easily oxidized in the atmospheric environment [6], and additional oxides may have been generated while the device underwent a period of time storage. Because oxides in the Schottky barrier may reduce the gate electric field across the channel, more gate biases are needed to pinch off the device, which results in shifts of V_{th} in the

Fig. 1. Schematic cross-section of the InAs/AlSb HEMT device.

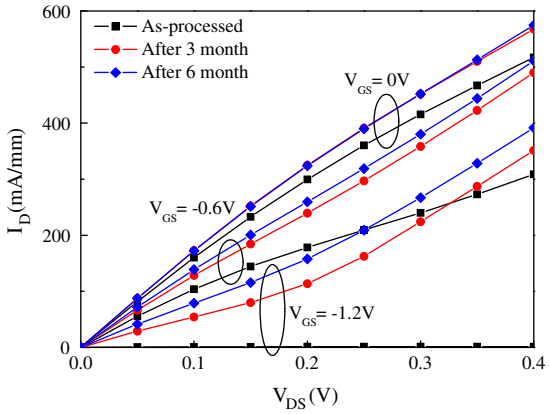

Fig. 2. Drain *I–V* characteristics of the device that had undergone different period of time in storage.

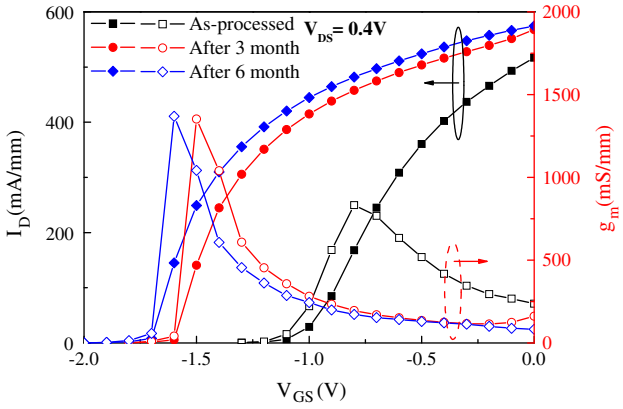

Fig. 3. Transfer characteristics of the device that had undergone different period of time in storage.

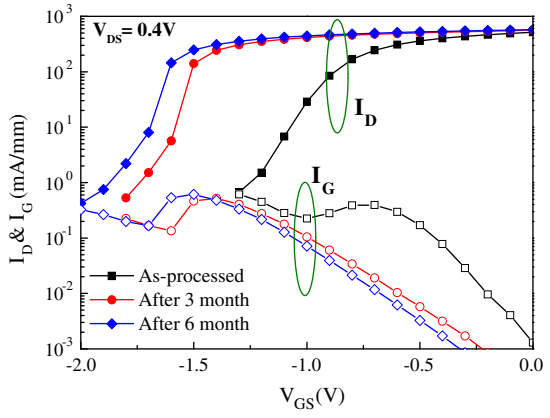

Fig. 4. Drain and gate sub-threshold characteristics of the device that had undergone different period of time in storage.