Solid-State Electronics 71 (2012) 63–68

Contents lists available at SciVerse ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

Behavior of triple-gate Bulk FinFETs with and without DTMOS operation

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ARTICLE INFO

Article history:
Available online 30 November 2011

Keywords:
DTMOS
Bulk
Triple-gate
Early voltage
Intrinsic voltage gain
Analog performance

ABSTRACT

In this paper, the combination of the Dynamic Threshold (DT) voltage technique with a non-planar structure is experimentally studied in triple-gate FinFETs. The drain current, transconductance, resistance, threshold voltage, subthreshold swing and Drain Induced Barrier Lowering (DIBL) will be analyzed in the DT mode and the standard biasing configuration. Moreover, for the first time, the important figures of merit for the analog performance such as transconductance-over-drain current, output conductance, Early voltage and intrinsic voltage gain will be studied experimentally and through three-dimensional (3-D) numerical simulations for different channel doping concentrations in triple-gate DTMOS FinFETs. The results indicate that the DTMOS FinFETs always yield superior characteristics and larger transistor efficiency. In addition, DTMOS devices with a high channel doping concentration exhibit much better analog performance compared to the normal operation mode, which is desirable for high performance low-power/low-voltage applications.

1. Introduction

FinFETs are attractive for advanced technology node applications such as analog circuits and SRAMs because of very good short channel effect control, higher integration density and ideal subthreshold slope [1,2]. These devices were originally designed on Silicon on Insulator (SOI) wafers. Several comparison studies in terms of performance have been performed for FinFETs fabricated on SOI versus bulk silicon substrates [3–8]. The Bulk FinFETs have advantages in terms of cost and defect density of the silicon substrate, heat transfer and compatibility with conventional planar CMOS devices.

The Dynamic Threshold voltage MOS (DTMOS) technique was first reported to improve the performance of planar devices [9]. This technique offers good perspectives as a low-power/low-voltage device because it provides improvement of the electrical characteristics and analog performance [3,4,10].

In the DTMOS technique, the body is tied to the gate terminal making the threshold voltage a function of the gate voltage. Fig. 1 shows the triple-gate Bulk FinFET structures and Fig. 2 shows the difference between the cross section of the channel regions of the Bulk FinFET and the DTMOS FinFET configuration.

Although the same idea can be used in planar technology, FinFET structures are attractive for the DT operation because these devices provide potential advantages that make them a possible successor to the planar CMOS technology.

In triple-gate FinFETs, with the influence of the three sides, the effective gate width of the transistor is equal to two times the height of the silicon-on-oxide layer plus the width of the silicon fin, $W = 2H_{Fin} + W_{Fin}$. The combination of a tri-gate architecture with DT operation is expected to result in excellent static and analog characteristics, corresponding with superior gate control for some range of fin widths. However, when the device becomes narrower, the lateral gates will take increasingly more control over the depleted body at the expense of the body contact so that the expected benefits of DTMOS operation will be gradually lost. It is the aim of this paper to verify the DT operation experimentally on devices fabricated in a Bulk FinFET CMOS technology and to compare the results with 3-D numerical simulations.

In the simulations, we used the appropriate physical mechanisms obtained from the experimental results. This way it is guaranteed that the simulated results are equivalent to the results of the experimental characterizations. The electrical parameters used in the simulation were obtained from the measurement results for undoped devices and the 3-D numerical simulator used is Atlas from Silvaco [11].

2. Experimental

The n-channel Bulk FinFET devices under investigation have 5 fins of 65 nm height (H_{Fin}) and are fabricated with extensions.

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doi:10.1016/j.sse.2011.10.022

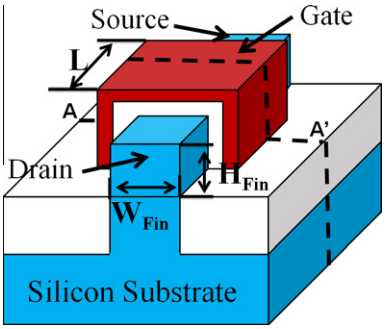

Fig. 1. Schematic view of a Bulk FinFET device (standard) indicating different device parameters like fin height H_{Fin}, fin width W_{Fin} and gate length.

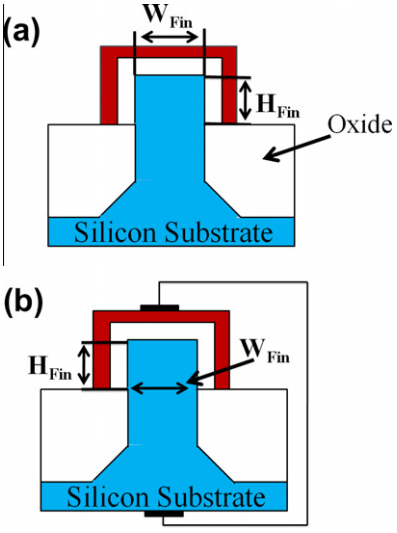

Fig. 2. Schematic representation of the channel cross section along the line A–A of the channel for a Bulk FinFET under standard biasing condition. Bulk (a); and DTMOS Bulk (b).

The channel is undoped and the gate dielectric consists of 2.5 nm of SiON capped with 5 nm Plasma-Enhanced Atomic Layer Deposited (PE-ALD) TiN and 100 nm poly-silicon. Well implants and ground plane doping were used to reduce the leakage currents between fins and transistors. The standard process flow up to metal 1 has been optimized for logic applications. More processing details can be found in [12]. Transistors with a fin width (W_{Fin}) of 40 nm up to 1 μm and channel lengths (L) varying from 180 nm till 10 μm have been characterized.

The simulated devices have an H_{Fin} of 65 nm and a fin width (W_{Fin}) equal to 130 nm. In other too see the better difference between Bulk and DTMOS FinFETs under analog performance, we choose $W_{Fin} \geqslant 130$ nm. For narrow-width the improvement due to DTMOS operation became smaller thanks to the better coupled side-gates. Both devices without channel doping (N_A) and with a channel doping concentration of 10^{18} cm^{-3} were simulated.

The drain current (I_D) and transconductance (g_m) versus gate voltage (V_G) are recorded at different drain voltages. The input characteristics in linear operation (V_D = 50 mV) and in saturation V_D = 1.2 V have been measured. The analog figures of merit are extracted at different bias conditions for the gate overdrive voltage (V_{GT}). Special attention is given to the Early voltage and intrinsic voltage gain, for which also simulations have been performed.

The subthreshold slope has been calculated by the minimum point of the $dV_G/d[\log(I_D)]$ curve and the threshold voltage is extracted by the Maximum Transconductance Change (MTC) method.

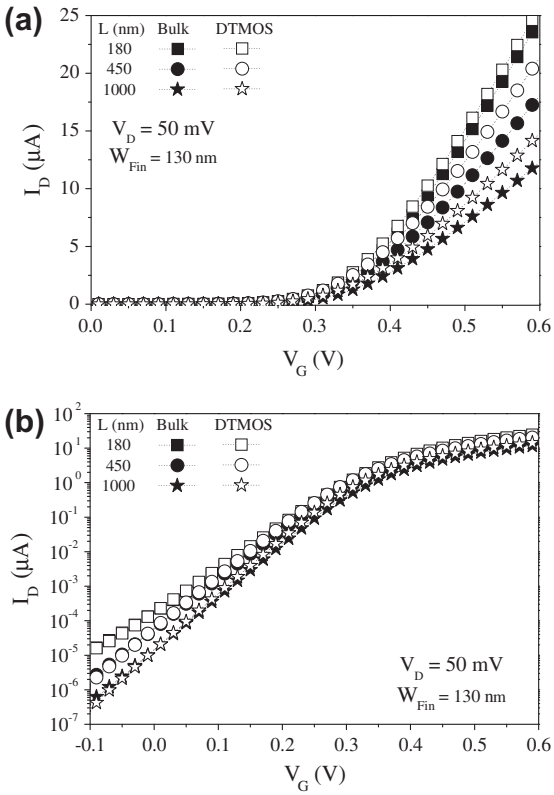

Fig. 3. Linear (a) and log scale (b) of experimental drain current (I_D) versus gate voltage (V_G) for Bulk and Bulk DTMOS triple-gate devices with different channel lengths (L).

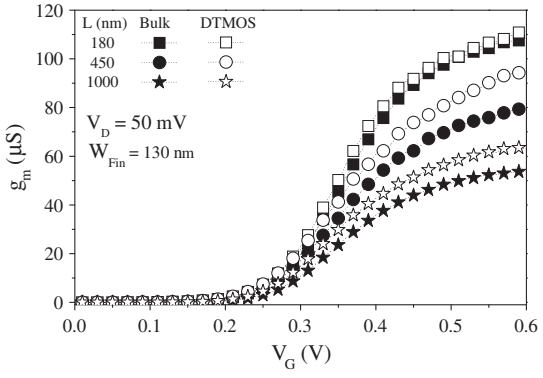

Fig. 4. Experimental transconductance (g_m) versus gate voltage (V_G) for Bulk and Bulk DTMOS triple-gate devices with different channel lengths (L).

According to this method, the threshold voltage can be defined as the gate voltage where the derivative of the transconductance ($dg_m/dV_G = d^2I_D/dV_G^2$) reaches a peak value, or, in mathematical terms, when $d^3I_D/dV_G^3 = 0$ [13,14]. This method was selected because it is appropriate to verify whether or not the devices have more than one threshold voltage (V_T) [15].

3. Results and discussion

3.1. Basic electrical characteristics

3.1.1. Drain current (I_D)

The drain current versus gate voltage is shown in Fig. 3 for Bulk FinFET and DTMOS FinFET transistors with different channel