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Monolithic 3D-ICs with single grain Si thin film transistors

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ABSTRACT

Monolithic 3D integration is the ultimate approach in 3D-ICs as it provides high-density and submicron vertical interconnects and hence transistor level integration. Here, high-quality Si layer formation at a low temperature is a key challenge. We review our recent achievements in monolithic 3D-ICs based on single-grain Si TFTs that are fabricated inside a single-grain with a low-temperature process. With the μ-Czochralski process based on a pulsed-laser crystallization, Si grains with a diameter of 6 μm are successfully formed on predetermined positions. Single-grain (SG) Si TFTs are fabricated inside the single-grain with mobility for electron and holes of 600 cm^2/V s and 200 cm^2/V s, respectively. Two layers of the SG Si TFT were vertically stacked and successfully implemented into CMOS inverter, 3D 6T-SRAM and single-grain lateral PIN photo-diode with in-pixel amplifier. Those results indicate that the SG TFTs are attractive for use in monolithic 3D-ICs on an arbitrary substrate including a glass and even a plastic for applications such as ultra-high-density memories, logic-to-logic integration, CPU integrated display, and high-definition image sensor for artificial retina.

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1. Introduction

Moore's law, which predicts doubling of density of integrated circuits (ICs) in every one and a half years, is approaching the fundamental physical limit. Furthermore, in the advanced IC, delay time is no longer limited by the transistors themselves, but rather by RC delay of the interconnects between the transistors [1].

Existent ICs are built using active devices within a single layer of Si. Additional layers above are used just for wiring or insulation. 3-D integrated circuits (3D-ICs) [2–4], in which active devices are vertically stacked upon each other separated by insulating layers, will break-through the problems of the conventional 2D ICs. Firstly, since the 3D ICs can stack many device layers, the integration density can be improved. This in turn brings a compact overall system. Secondary, short and dense interconnects will provide a short delay time in signal line and optimum routing capability, hence leads to a faster operation. Lastly the 3D-ICs can integrate more components with different functions in a chip, e.g., sensors, which increases the functionality, i.e., facilitating "More than Moore" approach in IC technology.

There are three different approaches towards the 3D-ICs: chip level [5], wafer level [6] or monolithic integration, as depicted in Fig. 1. Among the three approaches, the monolithic 3D integration allows transistor level integration and therefore provide the highest density of vertical interconnects between the stacked layers. Therefore the monolithic integration are suited not only for an ultra-high density memory or memory-on-logic but also for logic-to-logic and high resolution image sensor. Technical bottleneck so far in the monolithic 3D-ICs was, however, either the poor semiconductor layer quality or the necessity of using a seeding substrate.

We propose 3D monolithic ICs with single grain (SG) Si TFTs where transistors are fabricated inside a silicon grain with a low-temperature process. Location of the grain is accurately controlled by the μ-Czochralski process which is based on pulsed-laser crystallization and hence does not thermally deteriorate the underlying device layers. Single-crystalline Si wafers are not needed and therefore the process can be applied to a low-temperature resistant substrate, such as a glass or a flexible plastic.

In this paper, after reviewing current status of 3D-ICs and the μ-Czochralski process, fabrication process of stacking of two layers of single-grain Si TFTs will be explained. With two SG-TFT layers CMOS inverter, SRAM and lateral photodiodes with an in-pixel amplifier have been designed and monolithically stacked upon each other.

2. 3D-ICs: history and current status

Attempt to make the 3D integration already begun in 80s [7], driven by recrystallization of Si film, such as zone melt recrystallization (ZMR) [8]. The process, however, required a substrate temperature to be kept at around 1000 °C to help in melting the silicon directly underneath a heater for obtaining a high quality Si films. This results in contamination of the silicon layer and re-distribution of impurity profile in the existing bottom active

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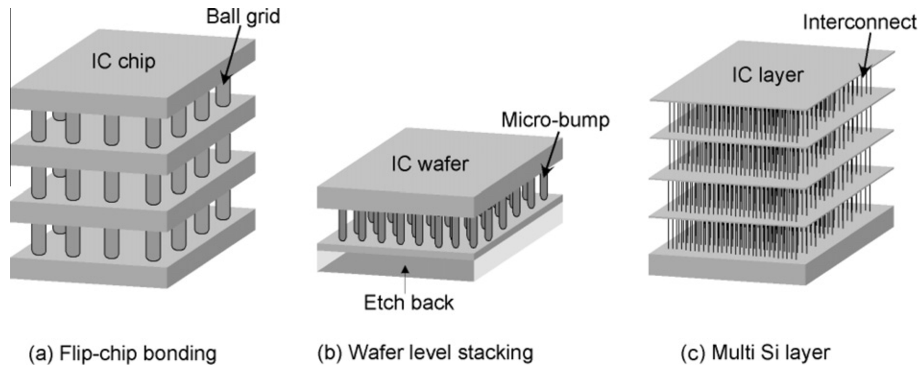

Fig. 1. Three different approaches for 3D-ICs: package (chip) level (left), wafer level (center) or monolithic (device) level (right) integration.

devices, apart from the slow process speed due to the low output power of the laser.

In the 90s, the chip-level integration made stacking of memory and logic devices commercially available mainly driven by the increased demand of small form factor [5]. Recently many research have been devoted for through silicon via (TSV) technology made with Cu in high aspect ratio via's which will allow more dense interconnections [9]. However, because the via size is inherently large with the TSV technology even using very thin Si substrate, application will be limited to only to the memory on logic or DRAM on NAND.

In the mid 90s, wafer level stacking technology [6] attracted for realizing of the 3D ICs. As shown in Fig. 1b, this technique basically uses layer transfer using bonding the pre-processed wafers, and then etching-back one of the substrates. Because it can utilize the single-crystalline Si layer and smaller interconnect size than the TSV, successful implementation of a multi-layer image sensor system with digital processing circuit has been demonstrated [6]. However, microbumps, which is used for metal joint between the interconnect, occupy a rather large area because the wafer alignment tolerance is in the order of microns. As a result, density of vertical interconnect between different layers of circuit is limited by the small number of the available bumps. Furthermore, the etching-back process in the wafer stacking technology posts mechanical damage to devices and cost to make this technology feasible.

The monolithic (or sometime referred as bottom-up wafer-scale) 3D integration allows us to make submicron size vertical interconnects therefore provide the highest interconnect density between the stacked layers. Here the Si layer must be newly formed on ILD at each level of the IC and therefore the crystalline quality of the layer is very important aspect for successful implantation. In the past, monolithic integration has been demonstrated with solid phase crystallization (SPC) [10–12]. While the process need a rather high temperature more than 650 °C, it has suffered a lot from the dense intra-grain defects which lower significantly the mobility. The process temperature can be further decreased to 450 °C by metal induced crystallization (MIC) [13] which uses a metal as catalyst. However, because of the poly-Si consists of needle-like grains, dense random grain boundaries (GBs) between the grains deteriorates mobility in the on-state and also create a leakage path in the off-state. Recently 3D SRAM has been demonstrated [14] with epitaxially grown Si from crystalline-Si substrate as seeds using laser crystallization. The process requires, however, high temperature (>600 °C) for the vertical epitaxial growth from the seeding substrate by solid-phase recrystallization and this will thermally deteriorate the underlying devices. CEA-LETI has demonstrated a monolithic 3D-ICs with a transferred, thin single-crystalline Si layer using a low-temperature molecular bonding of SOI substrates [15]. Owing to the thin inter-layer-dielectric (ILD) layer thickness of 60 nm, electro-coupling between the layers has been also demonstrated. Those two approaches, however, need obviously a single-crystalline Si or SOI substrate and therefore the application area is limited only to the micro-electronics and difficult to scale up to the large area electronics.

3. 3D-ICs with single-grain Si TFTs

Seen from the historical background, formation of high quality silicon layer with a low-temperature process is therefore a key challenge for realization of the monolithic 3D-ICs. The low-temperature is needed to ensure no thermal damage to the underlying device layer. In this regards, recrystallization with high power UV pulsed-lasers, e.g., excimer-laser, is suited for the 3D-ICs because the heat diffusion is limited to several hundreds nanometers due to the short melt/solidification event in the order of sub-μs, hence the bottom layer would not be deteriorated. The laser has been applied already for mass-production line of active matrix poly-Si TFTs backplane on a glass for flat-panel displays [16]. The problems of the laser crystallized poly-Si film is the small grain size and the dense random grain boundaries, which lowers channel mobility significantly [17,18]. However, if the location of the silicon islands is controlled, the position of the channel region of FETs can also be aligned inside the island. The 2D location control of Si grains can therefore eliminate inclusion of the random GBs and enables formation of single-grain (SG) TFTs.

So far very few have been reported the 2D location control of Si grains and formation of TFTs inside those. Among them the μ-Czochralski (grain-filter) process [19] has advantages in terms of the wide energy density window for obtaining the 2D location control, and the higher alignment accuracy over the other methods. As shown in Fig. 2, the process can grow large Si grain from "grain filter", which refers hole created in the underlying SiO_2 and filled with a-Si. Upon excimer-laser irradiation, the Si film surrounding the grain-filter melts completely, whereas the grain filter would not melt completely due to the large heat dissipation and heat capacitance there. During vertical growth of fine grain Si in the grain filter, occlusion of grains occurs reducing the number of growing grains. By increasing the aspect ratio of about more than 7, only single grain can be filtered out from the many pre-existing fine grains. The grain size can be up to 9 μm with optimization of the geometrical structure [20]. With a maximum process temperature of 350 °C, transistors that were fabricated inside a single, location-controlled grain (as schematically shown in Fig. 2b) exhibit mobility of 600 $cm^2/V\,s$ and 280 $cm^2/V\,s$ for electrons and holes, respectively [21]. Tensile strain can reduce effective mass and boost the both mobilities to 1.6 times [22]. An operational

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