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Epitaxial growth of Si:C/Si/SiGe into cavity formed by selective etching of SiGe

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ABSTRACT

Epitaxial growth of Si:C, Si or SiGe in the cavity formed by selective vapor phase etching of sacrificial SiGe layer by HCl using a RPCVD system was investigated. The sacrificial SiGe layer was etched with very high selectivity. Epitaxial Si was deposited into the selectively etched cavity by non-selective and selective deposition processes. Weak strain contrast was observed by TEM at the interface where the growthfronts from top and bottom of the cavity were meeting each other. No or weak strain contrast was observed in the Si cap layer at middle to shallow part of the cavity.

By non-selective SiGe growth, the SiGe layer was deposited on the Si cap layer only. The Si cap layer on the cavity seems to be bended and pressed down in the early stage of non-selective SiGe growth. On the other hand, in the case of selective SiGe growth, the cavity was filled. Strain contrast was observed by TEM in the Si cap layer on selectively grown SiGe. Bending of Si cap layer after selective SiGe growth was increased with increasing Ge concentration, indicating that tensile strain was generated by SiGe growth in the cavity.

1. Introduction

SiGe as sacrificial layer in combination with selective etching has been investigated because of its potential for various applications, e.g. for MEMS, for SON (Silicon-on-nothing) devices or for other new structures like nano-pipelines [1–3]. Different techniques have been applied for the etching of SiGe selectively to Si including electron cyclotron resonance (ECR) plasma etching [4], chemical etching [5] or microwave initiated etching using radicals [2] and conventional thermal processes [6,7]. The chemical vapor phase etching (CVE) process of Si is also applied for ultra-shallow junction formation by combination of Si CVE and selective SiGe growth [8].

In previous papers, we demonstrated selective CVE of poly-Si and SiGe by HCl using a conventional thermal process performed in a reduced pressure CVD (RPCVD) tool, which is also used for the deposition of the Si and SiGe [9–11]. So it is possible to combine sacrificial SiGe layer etching and the epitaxial layer growth in one process to prevent possible contaminations and additional bake before the epitaxial layer growth.

The motivation for this paper is to evaluate the possibility to perform epitaxial deposition within the selectively etched cavity and by this way to perform local strain engineering. The techniques for the carrier mobility enhancement by strained Si formed by SiGe or Si:C are widely reported [8,12,13]. In this paper, we focus on the growth of Si:C, Si or SiGe into the selectively etched cavity. By combining CVE and filling of the cavity by epitaxial SiGe layer, an approach for local strain engineering is discussed.

2. Experimental

Selective epitaxial growth (SEG) and non-selective epitaxial growth (NSEG) of Si:C, Si or SiGe into selectively etched cavity are carried out by using a single wafer reduced pressure CVD (RPCVD) system. For the sample preparation, 30 nm thick SiGe with 30% Ge content and 50 nm thick Si cap layer are deposited on Si(1 0 0) wafer at 600 °C and 700 °C, respectively. The Ge content of the sacrificial SiGe layer we used is 30% to achieve high selectivity of etchrate between Si and SiGe by CVE process [10,11]. Then a Si_3N_4 hardmask layer is deposited by CVD at 730 °C. After that the Si cap, SiGe and ~150 nm of Si substrate are etched vertically by ECR dry etching. In the case of NSEG to fill the cavity the Si_3N_4 hard mask layer which is used for the ECR dry etching is removed by wet etching. For the investigation of SEG to fill the cavity the Si_3N_4 hardmask was not removed and was used as a mask layer for SEG. After HF last clean, the wafers are baked at 800 °C in H_2 to remove the native oxide. Then selective CVE of SiGe by HCl is performed at 700 °C at atmospheric pressure. At this stage, XRD measurement in the non-etched area shows that the sacrificial SiGe layer was fully strained. After the CVE, Si:C, Si or SiGe are deposited by non-selective or selective processes in

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reduced pressure. No additional bake is performed between CVE and the Si:C, Si or SiGe layer growth. H_2 is used as carrier gas. SiH_4 and GeH_4 are used for NSEG at 500–700 °C. SiH_2Cl_2, GeH_4, and HCl are used for SEG at 700–800 °C. For Si:C deposition, CH_3SiH_3 is used as C source for both NSEG and SEG. Ge contents of SiGe are 10%, 20%, and 30% for NSEG of SiGe and 10% and 20% for SEG of SiGe. Ge and substitutional C concentration are measured by XRD using Vegard's law [14]. RCRefSimW software is used for the XRD rocking curve simulation [15]. Optical microscope, cross section SEM and TEM are used for analyzing the cavity after CVE and Si or SiGe growth. For the SEG of SiGe, the bending height of Si cap layer was measured. The bending height X of the Si cap layer, schematically shown in Fig. 1, is calculated with following formula:

$$X = T - (2 \times L) - D$$

T is the distance between the bottom of the Si_3N_4 hardmask and the bottom of the cavity. L is the thickness loss which is determined by the difference of Si cap layer thickness at shallow part of the cavity and the Si cap layer on the sacrificial SiGe layer. D is the thickness of sacrificial SiGe layer. The thickness loss of the Si substrate at bottom of the cavity is assumed as same as the thickness loss of Si cap layer.

3. Results and discussion

Fig. 2 shows the SEM image of the sample with a sacrificial SiGe layer containing 30% Ge after HCl CVE and after HCl CVE and NSEG of Si. The sacrificial SiGe is etched with high selectivity to Si (Fig 2a) [5,6]. After selective CVE of ~1.3 μm of the sacrificial SiGe the thickness loss of the Si cap layer is 6 nm determined by cross section TEM measurement. This means the ratio of the in-plane etchrate of SiGe with 30% Ge content and etchrate of Si perpendicular to Si (1 0 0) surface is more than 200. By combining HCl CVE and NSEG of Si, the cavity formed by selective etching is filled. No voids are visible in the cavity by SEM (Fig. 2b).

Fig. 3 shows cross section TEM images after HCl CVE and NSEG of Si and SEG of Si. By both non-selective and selective processes, Si layer is grown epitaxially in the cavity. No interface is visible between the cavity surface and the deposited Si layer. No O, C, and Cl peaks were observed by SIMS measurement of 6 μm square mesa checker-board structure. No crystallographic defects are observed in Si layer grown in the cavity. These results are indicating a low contamination level at the interface after CVE. The epitaxial Si layer is grown from both top and bottom of the cavity. Polycrystalline Si growth is observed on the sidewall of Si. The increased surface roughness of the sidewall caused by polycrystalline Si growth is also observed in Fig. 2a. The reason of the polycrystalline Si growth is not clear. A possible assumption is that residual contamination after ECR dry etching remained on the sidewall is preventing epitaxial growth. In the case of NSEG of Si (Fig. 3a–c), a thin and small void (1–2 nm) is observed at the deep part of the cavity (Fig. 3a). A possible reason of the small void generation may be slight bending of the Si cap during the Si layer growth. In the case of SEG of Si (Fig. 3d–f), a big void is visible at the deep part of the cavity (Fig. 3d). The thickness measured from the interface where growthfronts meet each other to the surface of the Si cap at shallow part (Fig. 3f) is slightly thicker than that at near the big void at the deep part of the cavity (Fig. 3d) indicating that the Si cap layer is slightly bended during the Si layer growth. For both NSEG and SEG of Si, strong strain contrast is observed in the Si cap layer near the void (Fig. 3a and d). At the middle to shallow part of the cavity for both samples after NSEG (Fig. 3b and c) and SEG (Fig. 3e and f) of Si, no or weak strain contrast is observed at the interface where the growthfront from top and bottom of the cavity are meeting each other. The contrast visible at the center of the grown Si layer may be caused by defect formation at the interface where the growthfront from top and bottom of the cavity are meeting each other.

Fig. 4 shows cross section TEM images after HCl CVE and NSEG of SiGe with 30% Ge content (Fig. 4a–c) and SEG of SiGe with 20% Ge content (Fig. 4d–f). The samples used for NSEG of SiGe (Fig. 4a–c) show thinner Si cap layer caused by CVE process. In the case of the samples for SEG of SiGe, the thinning of Si cap layer is prevented by the Si_3N_4 hardmask layer. After HCl CVE and NSEG of SiGe (Fig. 4a–c), a big void is observed at the deep part of the cavity (Fig. 4a) and almost no SiGe is grown in the cavity (Fig. 4a–c). SiGe is grown epitaxially on the Si cap layer. No dislocations were observed in the SiGe layer grown on the Si cap layer (Fig. 4a–c). Strong

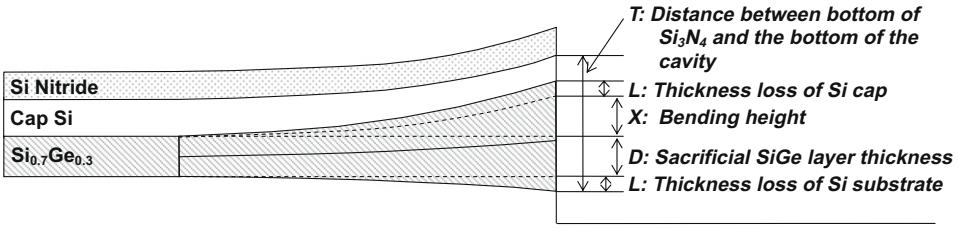

Fig. 1. Schematic diagram of the sample after CVE of SiGe and selective SiGe growth.

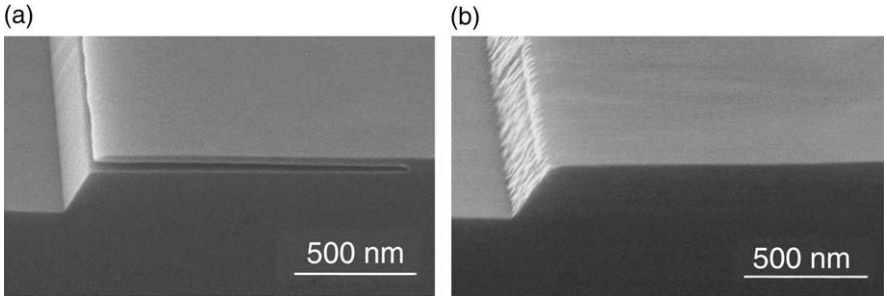

Fig. 2. SEM image of the sample without Si_3N_4 after: (a) HCl CVE and (b) HCl CVE and non-selective Si growth.